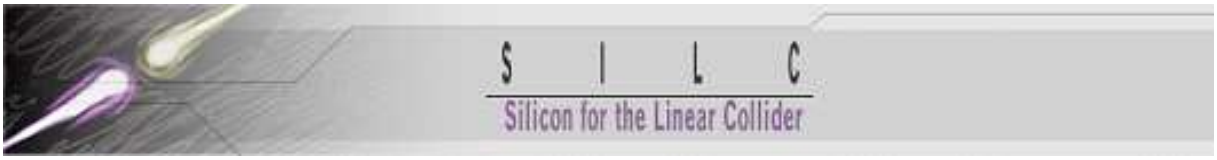

Status Report to the PRC DESY, April 1 and 2, 2008
Submitted on March 21, 2008, by

SiLC (**Si**licon Tracking for the **L**inear **C**ollider)

University of Michigan, LAPP/CNRS-IN2P3, University of Barcelona, IMB-CNM/CSIC, HIP University of Helsinki and VTT-Helsinki, IEKP University of Karlsruhe, Liverpool University, Moscow State University and SiLab, Obninsk State University, LPNHE-University Pierre and Marie Curie/CNRS-IN2P3, Charles University in Prague, SCIPP and University of California in Santa Cruz, IFCA-University of Cantabria/CSIC, Yonsei University, Korea University, Seoul National University, SungKyunKwan University, Kyungpook National University, INFN-Torino and University of Torino, IFIC CSIC–University of Valencia, HEPHY-Academy of Sciences in Vienna**.**

Abstract

This status report presents the main achievements of the SiLC Collaboration since2007. The previous results are reported in detail in the proposal to the ILCSC R&D Tracking Panel in February 2007. The main advances are on R&D on sensors especially on the baseline on new microstrip sensors, with the developed collaboration with HPK Photonics and with new firms interested in these new developments; the progress of VTT-Finland in making novel sensors based on 3D Planar technology; and the growing interest and participation of several SiLC teams to new pixel technologies. Another major breakthrough this last year is on the successful characterization of the new FE readout chip developed in 130nm CMOS UMC technology. It was fully tested at the test beam at CERN in 2007 together with the new HPK sensors. A new improved version of this chip including 96 channels with full digital managerial capability, calibration, power cycling is being submitted these next few weeks. It will equip the new prototypes for test beams. The hybrid alignment system has made major progress as well and is being implemented as a prototype in the test beam in 2008. Major advances in test beams have been achieved with the CERN test beam in 2007. This was the first combined test beam with the EUDET telescope. It will be pursued in 2008 with the first combined test beam with the LCTPC collaboration and the scheduled test beams at CERN in 2008. The collaboration is developing Silicon tracking prototypes for these various test beams. A task force on simulation has been launched this last year with the installation of all the components of the Silicon tracking system in the MOKKA framework, advances in the simulation of the very forward part on the digitization and reconstruction issues. The SiLC collaboration is preparing for participating actively to the LOI's scheduled for March 2009.

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Several members of the SiLC collaborations are members (HIP Helsinki, LPNHE Paris, Charles University Prague and IFCA Santander) or associated partners (IMB-CNM/CSIC Barcelona, IEKP Karlsruhe, University of Liverpool, State University of Moscow, State University of Obninsk, IFIC/CSIC Valencia, HEPHY-Vienna) to the EUDET, FP6 I3 E.U. project.
Several contracts between different partners of SiLC, these last years:
Contracts CICYT-MEC/IN2P3-CNRS between LPNHE and IFIC and IFCA
Contracts DOE of LPNHE with SCIPP-UCSC and SLAC or FNAL .
Contract France-Japan: LPNHE and KEK
Collaborative contacts with CERN (A. Honma and A. Marchioro)
Collaborative contacts with DESY (especially for the beam test infrastructures)
Collaborative contacts with B. Cooper and M. Demarteau at FNAL.

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Introduction

This status report presents the work achieved by the international R&D Collaboration, ***SiLC*** (**Si**licon tracking for the **L**inear **C**ollider) over this last year. This collaboration concentrates since several years on the developments of a new generation of Large Tracking systems based on the use of the Semi-conductor technologies. The first proposal was presented at the PRC DESY in May 2003 followed by an addendum in October 2003 [1]. A first status report was given two years later in May 2005 at the PRC-DESY [2]. The third status report to the PRC-DESY that was originally scheduled in May 2007, was postponed to this present session because of the presentation of the SiLC R&D to the Tracking session of the ILCSC R&D panel in February 2007 in Beijing during the BILC07 workshop [3].

This report refers to the work achieved after BILC07, i.e. starting January 2007, as the proposal presented for the review panel in Beijing gives a very detailed description of the ongoing R&D activities and the main results obtained at that date.

The first remark is that the R&D collaboration has not changed in terms of collaborating Institutions with respect to the ones listed in [3]. A new partner, the University of Barcelona, had just joined SiLC. Several teams have reinforced over this last year their contributions and the number of people involved in SiLC activities. This is mainly due to the termination of the construction work for LHC. For details on the present status of the Collaboration in terms of partners, their personal interests and expertise in the field, we refer to Part I of the Beijing proposal [3].

The Part I of this report presents in some details the advances over this last year in the various R&D objectives that are tackled by this collaboration. The main R&D objectives are focusing on the three basic topics: R&D on Mechanics, R&D on sensors and R&D on Electronics. It is followed by Part II which describes the tools the overall collaboration is developing. This includes especially the task force started after Beijing on simulations, the continuation of the active development of the Lab test benches and the test beam program that has been quite successful in 2007, with the start of the test beam activities at CERN and the first combined test beam with the EUDET vertex detector prototype. All these test activities are also closely related to the EUDET, E.U. Infrastructure Program under the FP6 E.U. program to which a part of the SiLC Institutes are directly participating. It must be noted that the outcomes of EUDET are at disposal of all the other SiLC collaborators including those from Asia and US. The EUDET memos for 2007 describing all the aspects of the SiLC activities in 2007 are largely referred to in this report.

The last part, Part III, discusses the participation to the overall ILC schedule with, in particular, the preparation of the detector LOI's and the future prospects.

[1] PRC R&D 03/02 and update 01/03 in http://www.desy.de/f/prc/html/documentation.htm
[2] PRC R&D 03/02 update 02/05 in http://www.desy.de/f/prc/html/documentation.htm
[3] SiLC proposal to the ILCSC R&D Tracking panel, BILC07, Beijing Feb. 2007 in: http://lpnhe-lc.in2p3.fr/DOCS/beijing.pdf

PART I: R&D main objectives

The SiLC collaboration is pursuing the R&D on the three main aspects: Mechanics, sensors and electronics. These three aspects are of course closely related and have as main goals to improve the detector performances in spatial and momentum resolution as well as in lowering the material budget and in still increasing the reliability and robustness of the overall system.

I-1: Mechanics R&D

Progresses on the Mechanics R&D have been achieved this last year mainly driven by the construction of prototypes for the test beams. The work focused on the development of the elementary modules, the construction of support structures for detector prototypes, the construction of a cooling prototype and advances in the alignment technique.

I-1-1: The elementary modules

A particular attention is devoted to the elementary module that will be the key piece or fundamental tile to build the overall detector architecture and to ensure the requested detector's performance from both mechanical and physics points of view. The main issues to be confronted are therefore to have a elementary module, easy to build and assemble, with an overall very low overall material budget (depending the location the aim is to have from 0.5% in the innermost region up to 0.8% in the outermost regions, all services included), possibly as unique as possible (avoiding the plethora of different modules depending the tracking component).

I-1-1-2 Modules built for the test beams in 2007.

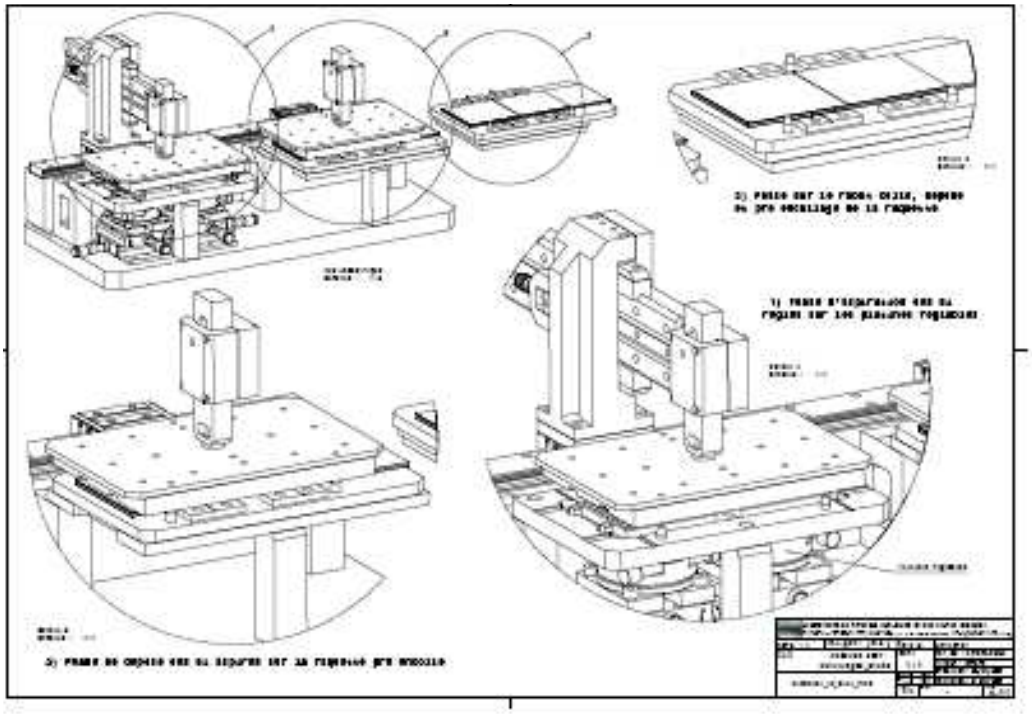
Two teams in the SiLC collaboration, IEKP-Karlsruhe and LPNHE-Paris have built several elementary modules that were used for the test beams in 2007.

IEKP has a strong expertise and all the needed developed tools for building these devices from past experience at CDF and CMS [3]. Karlsruhe built two modules for the test beams in 2007 and is presently in charge of constructing the modules for the combined test beam with the LCTPC (see also I-1-2-1). Here below are pictures of the tools presently used for this construction and of the modules already built or under construction.

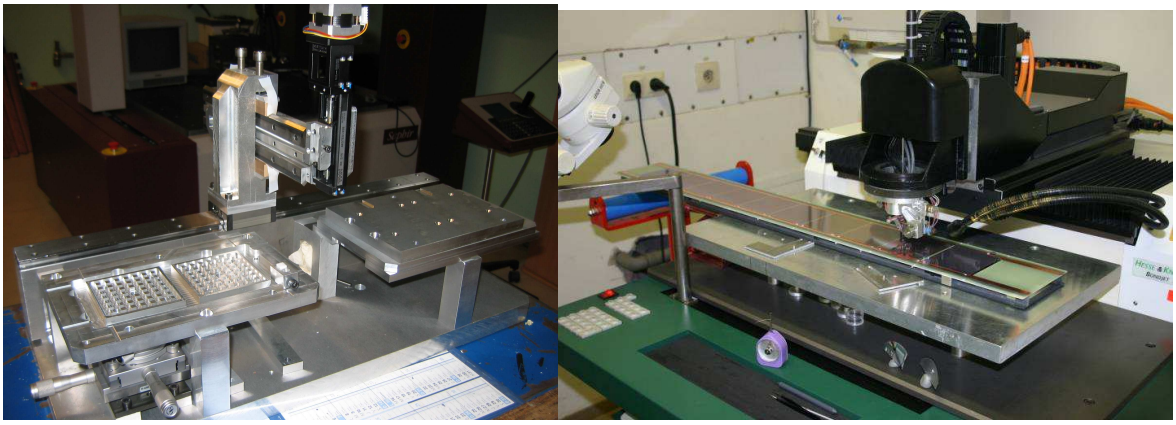
LPNHE is new in the field and is developing both the tooling and the expertise for constructing such devices. LPNHE built three modules for the tests in 2007 and is presently starting to build four new modules for the tests at CERN in 2008.

These modules are not yet the final ones foreseen for a future ILC detector. In particular the F.E. electronics are still in a hybrid board connected by wire bonding and through a pitch adapter to the sensors in so to speak a "classical way", presently used at the LHC. But the material and the supporting structures for the sensors are in the way to minimize as much as possible the material budget, one of the major goals of this R&D.

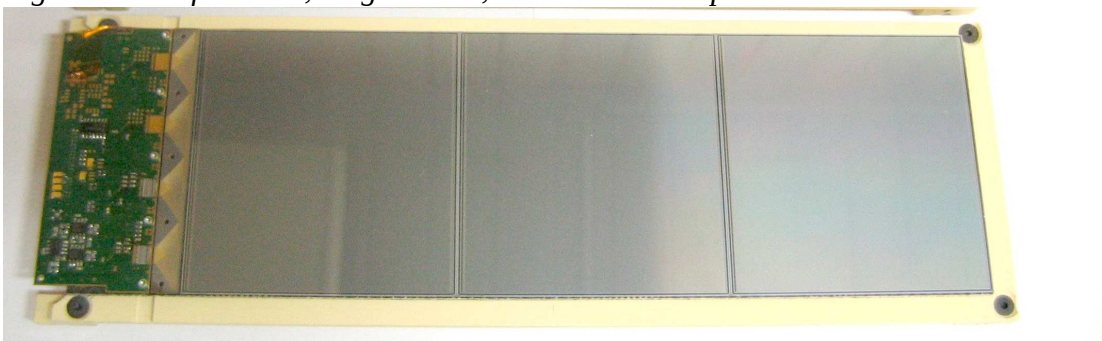
The FE boards were developed at LPNHE and were wire bonded to the modules by the bonding Laboratory of M. Moll and collaborators (A. Honma and McGill) at CERN.. The CERN team was instrumental to the realization of these modules.



Design of the tooling for building the elementary modules at LPNHE



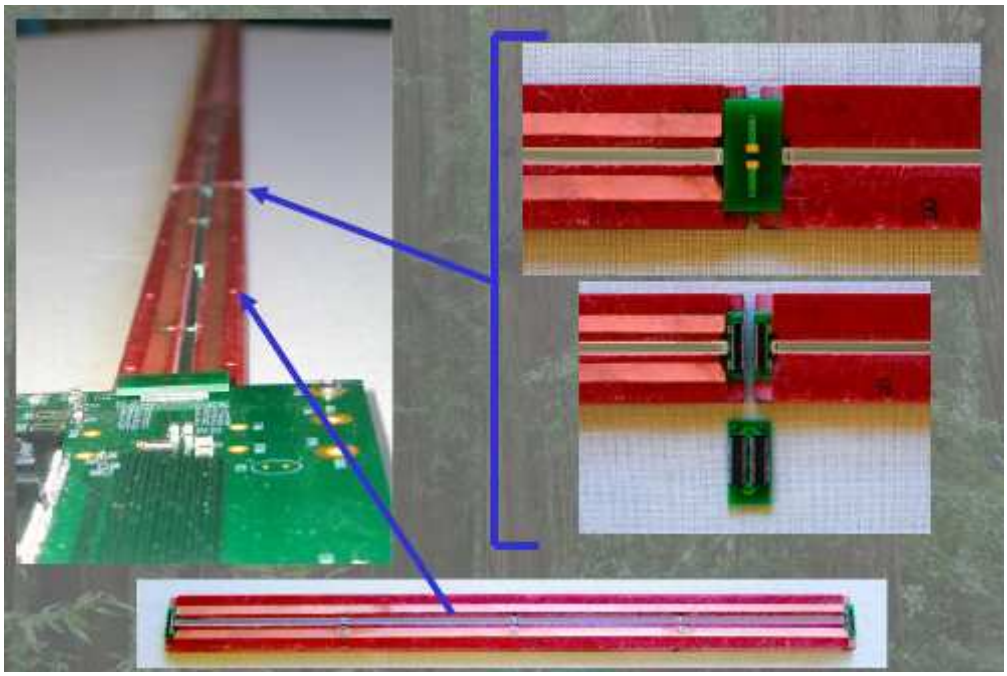
On the left, photograph of the tools to build the elementary modules made of two sensors, at LPNHE, realized according to the design shown in the schema here above.
On the right, the photograph of the machine available at IEKP for building modules even with a large number of sensors, long ladders, as shown in this picture.



Photograph of one of the first elementary modules made of 3 sensors with the pitch adapter and the hybrid card instrumented with 4 VA1 chips, used at the DESY and CERN test beams in 2007 as reference module.

I-1-1-2 The long Ladders

SCIPP and UCSC are promoting the use of long ladders and have built such devices using GLAST sensors with large readout pitch or sensors as those of Layer 0 in the CDF experiment, therefore with small readout pitch.



Long ladder built by SCIPP

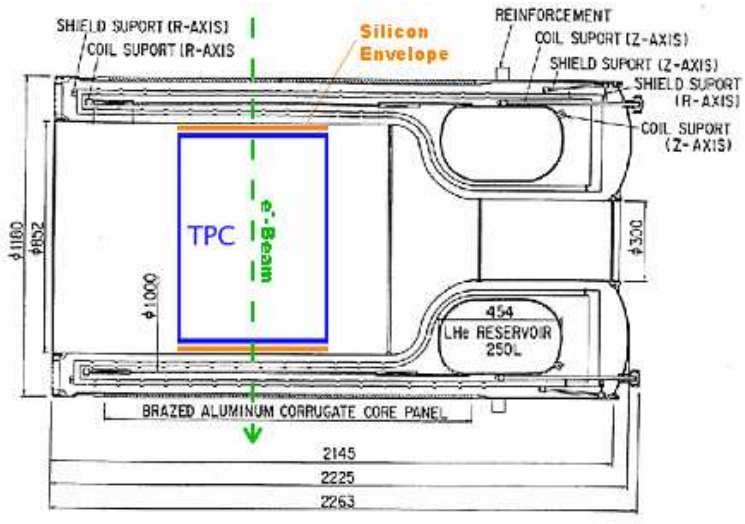
Several other Institutes, member of the SiLC collaboration have the facilities to build elementary modules e.g. IFIC and Liverpool University.

I-1-2: Construction of prototypes and needed tooling

The design and construction of two prototypes has been performed in 2007 for the test beams scheduled in 2008 and 2009.
One prototype is a prototype of the Silicon envelope for the TPC in the LDC detector concept. The other one is the 4-layer prototype that will serve for the development of the Silicon layers both for the end plug layers (XUV type) and the barrel Silicon layers.

I-1-2-1 The Silicon prototype for the LCTPC

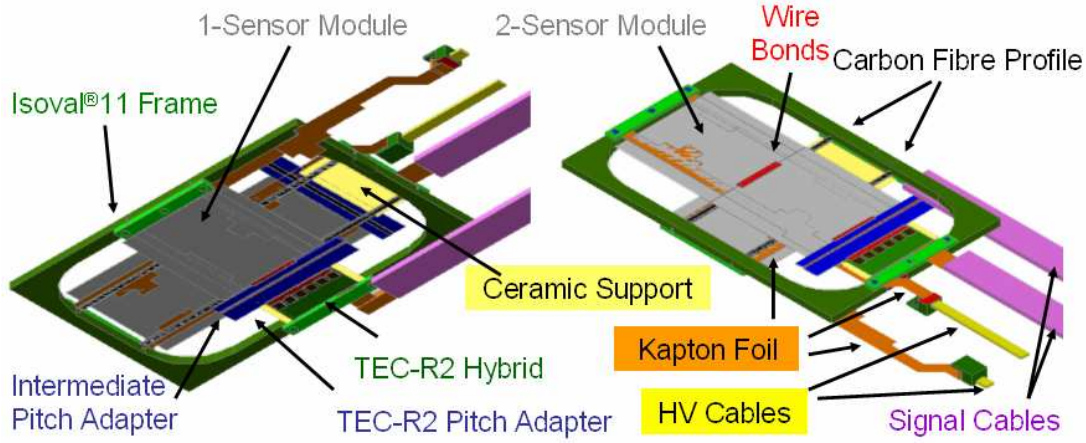
The Linear Collider TPC (LCTPC) collaboration is formed of several groups. Their goal is to evaluate different TPC designs for the ILC.
This collaboration has invited at the end of 2006, the SiLC collaboration to join them in a combined test beam set-up that will be a prototype of the proposed Silicon layers (also called Silicon Envelope) surrounding the TPC. Three teams from The SiLC collaboration are presently involved in the preparation of this prototype: HEPHY Vienna (sensors and APV25 readout), IEKP Karlsruhe (construction of modules and of the support structure), LPNHE Paris (new chip readout SiTR_130-96)



LPTPC test beam setup at DESY

The current test-beam setup at DESY consists of a TPC (in blue) inside a superconducting magnet called PCMAG. Silicon modules (orange) inside the magnet are provided by the SiLC collaboration [4]. They will provide very precise 3D points just outside the TPC and will work as telescope for the track reconstruction. The point resolution of the silicon sensors will be better than 15 µm in phi and 15 µm in z-direction. This is possible by using two silicon microstrip sensors with very narrow pitch crossed at an angle of 90 degree. Only four silicon modules two in front and two behind the TPC, with respect to the e^--beam, will be installed. On each side of the TPC, a support frame will hold two modules, where one module consists of two daisy-chained sensors while the other module is installed perpendicular and consisting of one sensor only.
Since the magnet will be moveable w.r.t. the beam and the TPC will be moveable inside the magnet the modules have to compensate these movements to keep the readout areas inside the beam spot. In addition the two modules have to move independently from each other to compensate different deviations of the beam due to different magnetic fields. This, and the very limited space, makes the design of the modules and their support very challenging.

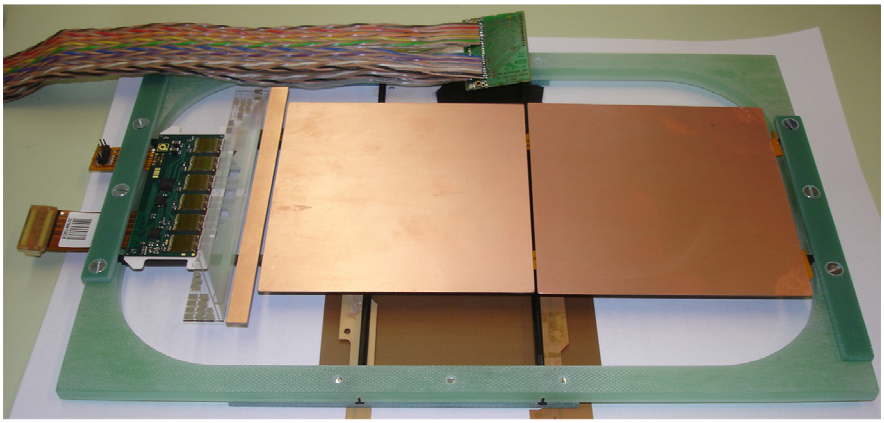
Thus, two one-sensor and two two-sensor silicon microstrip modules will be built. They get mounted in pairs onto an Isoval®11 frame, as shown in the picture below.



The sensors have been manufactured by HPK according to a design of the SiLC collaboration with a thickness of 320 µm and a size of 91.5 mm x 91.5 mm. They have 1792 readout strips with a strip pitch of 50 µm. In the first setup only 768 of these channels will be read out

reducing the readout sensitive area to 38.4 mm width, since front end (FE) hybrids leftover from the CMS Tracker End Cap module production will be used in the beginning. Later on, these hybrids will be replaced by others containing newly developed SiTR_130 FE chips.

The CMS hybrids are already connected to the appropriate pitch adapter for specific sensors with a pitch of 143 μm. Since it is impossible to remove this pitch adapter (PA), an additional PA has to be designed. This so-called intermediate PA connects 768 channels with a pitch of 143 μm on one side and a pitch of 50 μm on the sensor side. It is currently being built in two different versions, on a 4-layer printed circuit board (PCB) and with Aluminium on quartz. The backbone of each module consists of two carbon fibre T-beams. For mechanical studies, a nun-functioning design study has been built (see picture below)

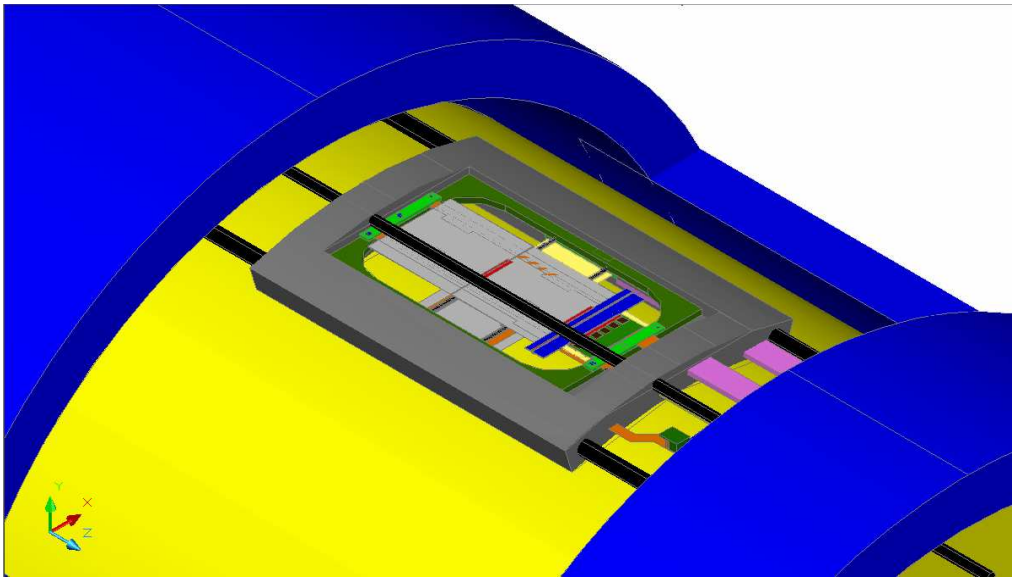


Photograph of the mounting of one of the Silicon module for the LCTPC test

Since there will be a shutdown at DESY in the first half of 2008, the test beam will not be available before August 2008. It was decided to use the time before to perform first tests with cosmics. For the cosmic run the design of the silicon envelope has to be changed:

1) the modules will be installed at the top and bottom of the TPC which interferes with the support plates of the TPC
2) for this setup the sliding carriage for the silicon envelope only needs to be moveable in z-direction, to move the silicon envelope inside the gap between the magnet and the TPC and out again. (the phi movement and hence the curved rail system is not needed)

No changes are needed on module level. The cosmic run is a great possibility to make first experiences with the modules, the readout system and a simplified module support system. A sketch of the cosmic run setup can be seen below, showing the silicon modules located between PCMAG magnet (blue) and the TPC field cage (yellow).



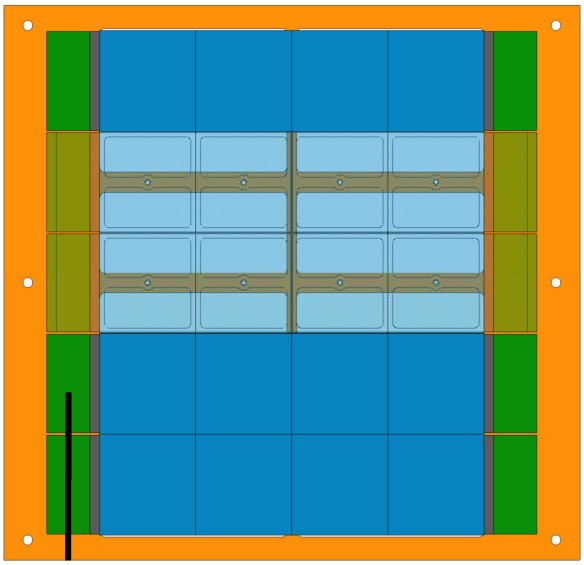
Artisitic view of a set of two Silicon modules giving the XY coordinates as prototype of the Silicon envelope to the TPC mounted on a supporting structure around the TC prototype

According to the schedule, the first cosmics will be measured in summer of 2008. The following months will be used to fully understand the readout and to combine the XDAQ readout system with the TPC system to provide tracking information. In fall 2008 the silicon modules will be installed in the original position inside the beam line with the final version of the sliding carriage that enables additional phi movement of the modules. Additionally, it is foreseen to replace parts of the CMS readout system with newly developed electronics containing the SiLC readout chip in the future.

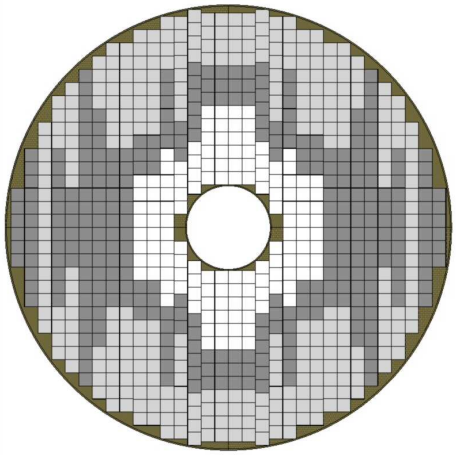
[4] EUDET-memo-2007-28, *SiLC Sensors for the Large Prototype TPC at DESY*, S.Haensel, T.Bergauer, M.Dragicevic et al. in http://www.eudet.org/e26/e28 and references therein.

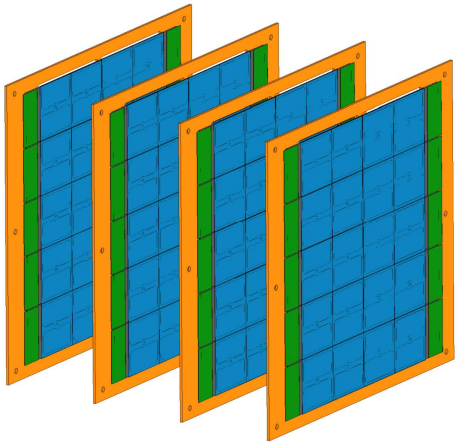
I-1-2-2 The 4-layer prototype

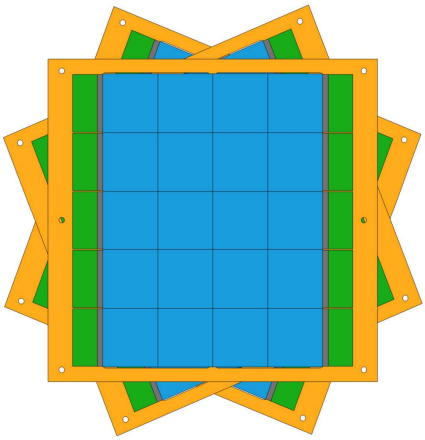
Based on the CAD drawings for the external Silicon layers and for the XUV layers of the end plug Silicon component described in [3] and as shown in the CAD design here below, a set of four layers is under design and construction for the combined test beam in 2009 at FNAL (see section II-2).
These layers are each made of 2 modules x 5, i.e. ten modules, with 2 sensors per module. The construction of these layers of which one will be achieved in 2008 will first allow studying all the issues related to the mounting of a support structure with fully equipped Silicon detectors. It thus includes not only all the alignment issues, mechanical robustness, reliability and reproductivity but also cabling, cooling issues etc…The modules mounted on the first layer will be built still in the standard way, i.e. with hybrid boards for hosting the FE readout electronics. The sensors are new HPK sensors [see I-2-1]. The next layers (2009) will be equipped with other sensors and with chips bump bonded onto the sensors themselves at least for part of them if the developed technique is proven to work (see I-3)



Prototype of one part of one layer of the end plug Silicon tracker (CAD here above)







On the top left, a CAD design of one layer with 10 modules (typically 60x55cm^2 all included); on the top right a CAD design of one of the XUV layer for an endcap component. On the bottom left, the 4 layers are arranged as in a central barrel Silicon tracking prototype; on the bottom right 3 out of the 4 layers are arranged in a XUV tracking end plug prototype.

I-1-3: Alignment systems

Precise alignment and positioning are crucial systems in order to be able to build and to achieve the very high spatial resolution performances requested for such detectors in the ILC environment. Adding the smallest possible material budget in the overall tracking system is another crucial issue.

The SiLC collaboration is considering two alignment systems

- The ***Frequency Scanned Interferometry (FSI) system*** as developed by the University of Michigan at Ann Arbor. This is the system that was considered since the beginning by SiLC (see proposal and status reports to the PRC-DESY) and it is indeed pursued by our collaboration.
- The ***hybrid approach*** developed by the IFCA/CSIC-University of Cantabria is part of the EUDET E.U. program of SiTRA. It is based on the existing expertise on alignments system of the IFCA team as well as on their learning experience at the CMS experiment.

The FSI system aims to have much below the one micron resolution accuracy, while the hybrid approach should succeed to get 2 to 3 microns resolution. Comparison of these two systems on realistic basis, i.e. when included as prototypes in a test beam and possible complementarities will be part of the tests as well as of foreseen simulation studies, SiLC will undertake with those two systems in these two next years.

Hybrid approach: Integrated co-linearity monitors and offline track alignment.

During year 2007 a great progress in the understanding of the behaviour of the silicon microstrip detectors as an optical multilayer has been achieved. First steps towards the production of Si microstrip detector prototypes have also started. The access to CNM infrastructure plus co-work with members of CNM has been crucial in the achievement of a number of goals summarized herein. In short, we present progress in 3 fronts:

- Realistic simulation of a Si microstrip (photo-)detector and study of thickness tolerances for its fabrication
- Optical characterization of detector materials
- Transmittance of Si as a function of doping

Detailed information on the different topics can be found in two EUDET publications [5], [6].

1.- Optical simulation of real Si microstrip detectors

Provided the refraction index and thickness of the layers of a multilayer media are known, the theory of multiple reflections accurately describes the balance of transmitted, absorbed and reflected light for the stack. Starting from this situation in early 2007, we arrived to a realistic model of the sensor where effects as the segmentation of the strip layer (and implants bellow it) are simulated taking into account the effect of the beam diffraction [5]. In order to cross-check this simulation, CNM provided us with a wafer of strip detectors, 80 μm pitch (see bottom wafer in figure here on the front right).

Top left: Undoped Si with SiO2 and Si3N4. Left to right, top to bottom: same as before but with increased doping level. Bottommost sample contains small samples of microstrip detectors

1.1- Fabrication tolerances

Silicon displays moderate absorption in the NIR range, slightly above its bandgap ($\lambda > 1$ μm). Thus, laser beams above that wavelength are able to traverse ~300 μm of Si. The rest of layers of the sensor have thicknesses comparable to this wavelength. That is the reason why small changes in the thickness of the materials can have an impact in the overall transmittance of the detector. A dedicated meeting with CNM clean room specialists and our in-house contact persons was hold at CNM in order to clarify deposition and oxidation tolerances of the different materials. As an outcome of the discussion we improved our simulation achieving a detector design that delivers maximum

transmittance within real fabrication tolerances. The performance of the detector has been calculated (using Monte Carlo techniques to degrade less than 10% of the maximum).

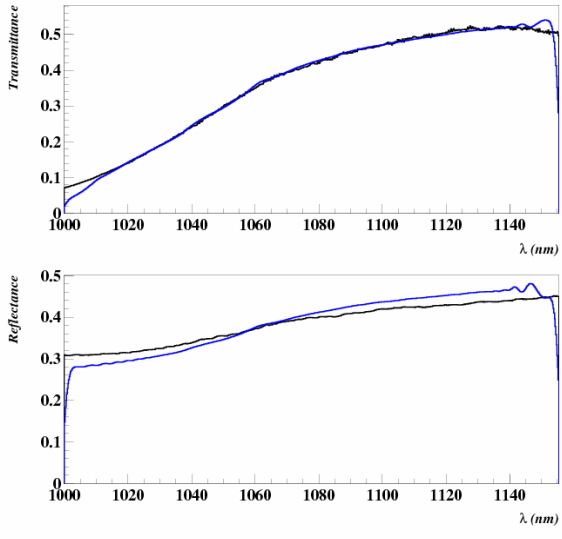
2.- Optical characterization of detector components

All the results calculated with the simulation have been obtained using refraction indexes (variable with the wavelength) from bibliography. Prior to the production of the first prototypes, we needed to characterize optically the materials as produced by CNM. Refraction indexes can be easily obtained from thin films samples of the materials. We decided to deposit one layer of material at a time on each of the 4 quadrants of a wafer. Four different wafers were used for this test (see 2 top rows of Figure above), each with different combinations of Si doping (explained in next section) plus 0, 1 or 2 layers of material above. The samples were delivered on the second week of January 2008 and the measurements are currently being analyzed.

3.- Effect of doping on Si optical properties

Optical properties of doped Si are reported to be very different from intrinsic Si (see for instance [7]). In that reference it is shown that the optical absorption coefficient (a measure of the attenuation of the light intensity per unit length of material crossed) raises exponentially as the doping concentration increases. In order to crosscheck these measurements, we have doped 4 double-polished wafers with increasing doping concentrations (picture of wafers in Figure above). To avoid unnecesary opacity of the wafers to NIR light, the implantation depth was approximately 1-2 µm from the Si-air interface.

The wafers, produced at CNM, within the GICSERV access framework, have been measured with a grating spectrometer 1.2 nm spectral resolution operating in the wavelength range 950-1150 nm. Contrary to what was expected, and although these measurements are still being analyzed, the effect of doping does not seem to affect in the optical transmittance of the samples. Very preliminary results are shown in the figure here on front right.



Preliminary comparison between the measured transmittance and reflection of Si as a function of the wavelength (black line) and optical simulation (blue line)..

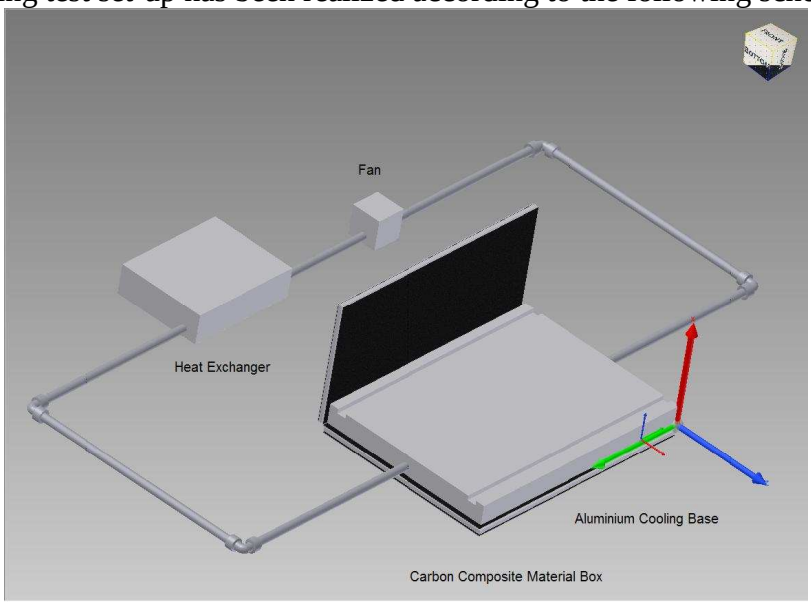
A retrospective balance of this year has shown us that there was a long way to go from the ideal simulation of the detector to a realistic one. This prevented us from processing samples in the clean room at CNM before the facility was closed for the upgrade. But, on the other hand, this allowed us to develop further our understanding of the sensor, address specific problems before they could happen (deposition tolerances is an example) and gain expertise and know-how on the processing steps and fabrication methods in the clean room.

References

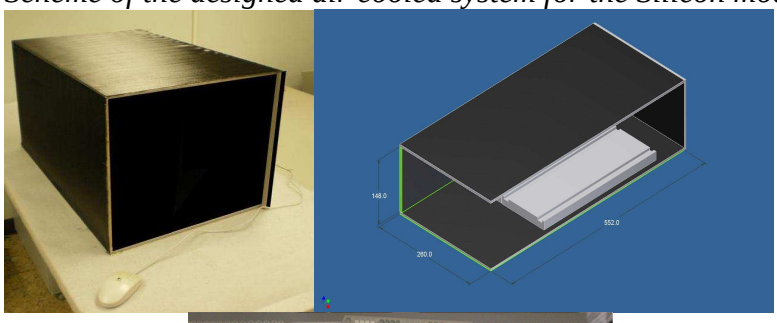
[5] M. Fernandez, G. Pellegrini, M. Lozano, I. Vila et al., EUDET-Memo-2007-32, "*R&D on Microstrip IR Transparent Silicon Sensors*" in http://www.eudet.org/e26/e28 .
[6] M. Fernandez, G. Pellegrini, M. Lozano, I. Vila et al., EUDET-Memo-2007-31 "*JRA2 SiTRA Alignment activities during 2007*" in http://www.eudet.org/e26/e28.
[7] S. E. Aw, H. S. Tan and C. K. Ong, J. Phys. Condens. Matter 3 (1991) 8213-8223.

I-1-4: Cooling system

The cooling prototype system was a deliverable of the EUDET project. Such a prototype has been realized by the OSU team [8]. A detailed study was performed and is reported in the EUDET memo [8]. It follows preliminary studies on mechanical prototypes performed by LPNHE mechanical team and also on the results on power dissipation of the first SiTR_130 prototypes. The measured power dissipation does not exceed 1mW per channel without power cycling. The main effect to avoid is the power dissipation due to the neighbouring devices and thus the cooling frame will mainly serve as an insulating frame from the external nuisances both from thermal and electrical origins.
The possibility of air cooling has been included as well just in case it is really needed.
An air cooling test set-up has been realized according to the following scheme



Scheme of the designed air cooled system for the Silicon modules



The insulating frame (see photograph on top left and design and top right) is built in a new composite material, namely double sided honeycomb Carbon composite material (see photograph of a roll of this material here above), which is a low material budget with all the mechanical and thermal requested properties [8].

[8] EUDET-Memo-2007-52, *Air Cooling of Silicon Strip Test Setup for a Linear Collider Experiment,* A. Savoy Navarro, A.Galkin, V.Saveliev, in http://www.eudet.org/e26/e28.

I-2: New sensors R&D

The SiLC R&D collaboration is benefiting from a large expertise and also good contacts with several founders. Besides there are some Institutes like HIP (with VTT) or Korean Universities (with ETRI) that are in close collaborative contacts with a firm or which have the needed facilities for doing themselves R&D on sensors (IMB-CNM in Barcelona). Moreover another asset of our collaboration is the expertise developed by HEPHY Vienna and IEKP Karlsruhe, in developing dedicated test benches for Quality Control Test in close collaboration with the vendors as Hamamatsu HKP and ST Microlectronics for CMS experiment.

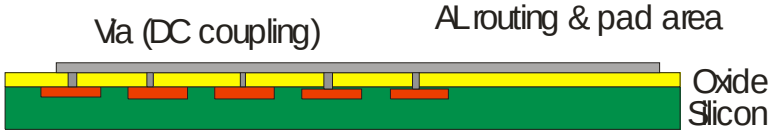
An organized effort has thus been launched and is coordinated by HEPHY.

I-2-1: The microstrips baseline

A baseline sensor design has been established to get comparable results from different sensor producers. Since future silicon strip sensors for the ILC will need a very high resolution, a readout strip pitch of 50µm is foreseen, possibly with intermediate strips in between, resulting 25µm pitch. The sensor bulk material is agreed to be p-on-n float zone silicon. The bulk material should be of high resistivity (5-10 kΩ cm) and rather thin (100-300µm). However, the lower limit of the thickness is limited by the noise figures of the readout chip. The detector must have a very low dark current of <1nA per strip, since the noise is mostly defined by the dark current and bias resistors. This implies very high values for the bias resistor in the order of 20 to 50 MΩ, realized either using poly-silicon, punch-through or FOXFET technique. While poly-silicon is more radiation hard, PT or FOXFET would be cheaper.

For the inner silicon layers, we propose AC coupled double sided detectors made on 6" wafers, while for outer layers, larger wafers of 8" or even 12" inch would be needed to reduce the material necessary for mechanical support. In this region, we propose single sided detectors preferable DC coupled for cost reduction

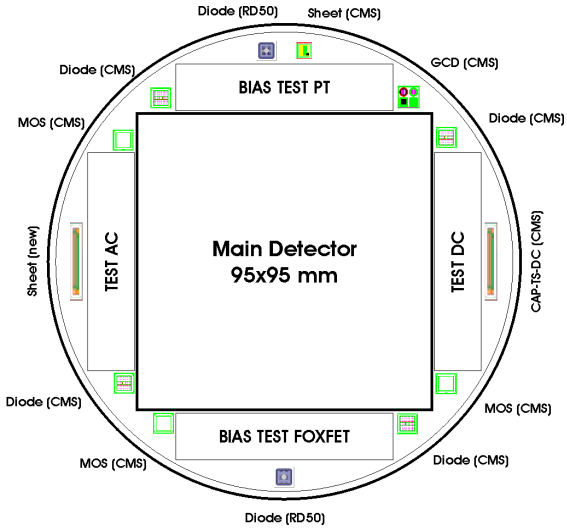
Since multiple scattering is a crucial point for high-precision ILC experiments, the amount of material inside the detector must be kept on a very low level to avoid degradation of the feasible resolution of the devices. The most radical solution is to integrate the pitch adapter completely into the sensor. The connectivity of the strips to the readout chip can be made by an extra metal layer for signal routing which is separated from the strips using an additional oxide layer. In this scenario, the readout chip can be bump-bonded onto the sensor as for pixel detectors. This is shown in the following figures.



The SiLC collaboration is in contact with different sensor producers and has already started to collaborate with them to produce the first prototypes according to the first step of the work program. Only vendors which are willing to collaborate and to provide sensors and test structures now are considered for the future parts of the work program.

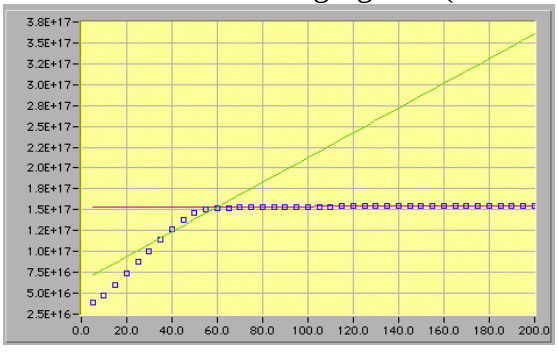
One batch of silicon sensors has been ordered at Hamamatsu Photonics (HPK) in Japan. This order consists of 30 normal sensors plus 5 “alignment sensors” which have a hole in the backplane metallization to allow laser light to pass through the silicon.

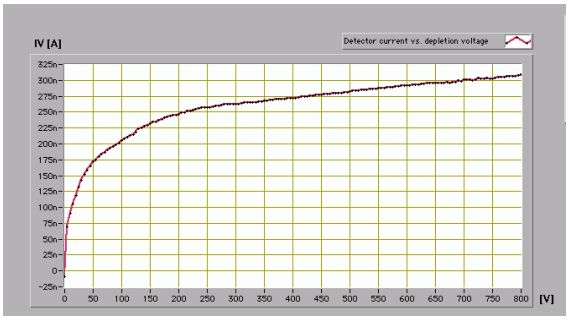
The layout of the Detector was design by the SiLC collaboration together with HPK and the result is shown in the following figure.



It is a single sided AC coupled strip detector with a sensor size of 91.5 x 91.5 mm² and a thickness of approx. 320 µm and agrees in all points to the sensor baseline defined above.
Various small test structures have been placed around the main detector on the wafer, e.g. diode, MOS, gate controlled diode, and others. Four large test structures have been designed with two different purposes. Two structures comprise 256 strips with the same pitch as the main detector, but with regions of different strip widths and different intermediate strips. Each region consists of 16 individual strips with the same geometry. Both structures will be used to test cross-talk and inter strip capacitances in a test setup and the resolution in a future beam test. The two other test structures on the wafer take advantage of different biasing schemes and have been designed to test FOXFET and punch-through biasing methods.

We received the sensors in October 2007 and first measurements have already been performed. The results are as expected for the resistivity and the dark current behaviour. This is shown in the following figures: (CV curve left, IV curve right)





Both, resistivity and dark current meet the requirements. On one sample of the sensors, a full strip scan has been performed as well. It consists of the determination of the single strip dark current, the poly-Si resistor value, the coupling capacitance and the dielectric current. These measurements are repeated for every single strip. The results show that the sensor is well within the specified limits [9].

VTT (*Valtion teknillinen tutkimuskeskus*) is a large technical research center in Finland. The goal of the collaboration is the development edgeless detectors (see I-2-2).

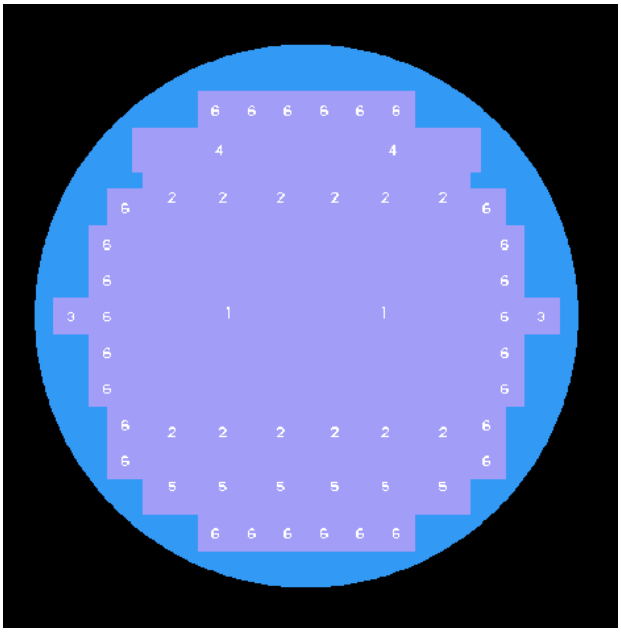
One of the goals of the SiLC collaboration is to establish companies to deliver silicon detectors for future HEP experiments. With this in mind, new fruitful collaborations started not only with HPK and VTT but also with ON Semi and IET with very promising results, which allows us to go to the next step with these vendors very soon. This helps to establish the procedures, processes and contacts with the producers very early to have a good basis for future steps. Other vendors willing to cooperate in the future have to fulfill the same requirements which these vendors already passed.

The next goals are the development of sensors with dual metal layer structure for in-sensor routing. Together with this, a cheap, industrial bump-bonding technology must be established to take full advantage of this technique. In parallel, sensor producers will be encouraged to build doubled sided detectors, together with evaluation of companies capable of 8" inch or even larger wafers.

[9] EUDET-Memo-2007-27, *Generic Silicon Strip Detector R&D*, T.Bergauer, M.Dragicevic, S.Hänsel, M.Krammer et al., in http://www.eudet.org/e26/e28.
[10] Th. Bergauer, *Silicon Strip Sensor R&D and results from HPK sensor measurements*, presented at the Sixth SiLC Workshop in Torino, University degli Studi, Italy, Dec 2007 (http://www.silc.to.infn.it/doc/papers/) and at the TILC08 Workshop, March 2008 in Sendai, Japon (http://www.awa.tohoku.ac.jp/TILC08/, see program)

I-2-2: The novel sensor technology: Planar-3D detector

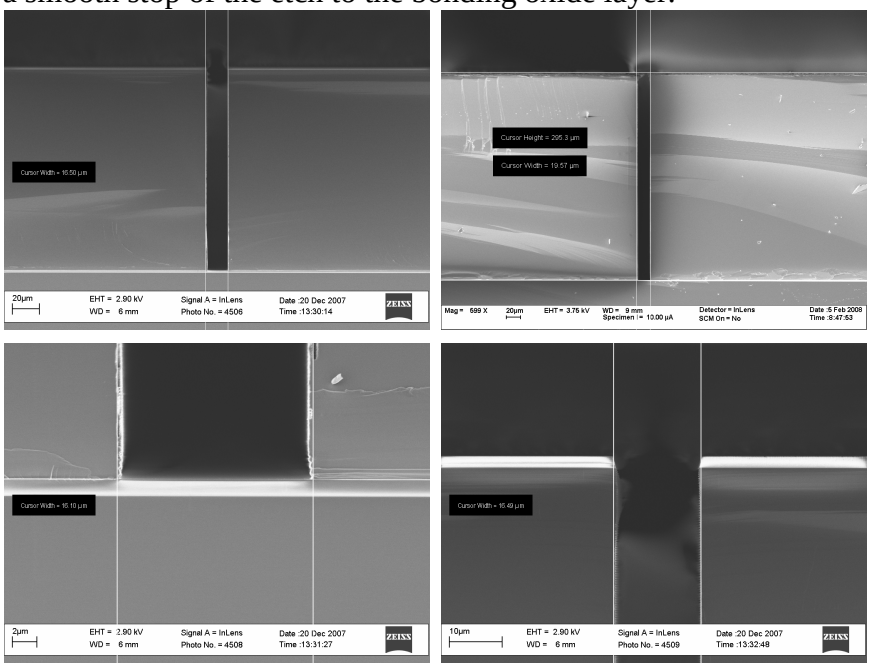
The planar-3D detector design offers some attractive properties for the ILC. When bonding sensors to make one module, the planar-3D design reduces the insensitive area between sensors. These sensors can be made very thin and the active edge avoids inhomogeneous electric fields and surface leakage currents [11].
The detector includes two main sensors with 5 x 5 cm^2 on 4" wafer, one DC coupled and the other one AC coupled with FOXFET biasing. These sensors are labeled with (1) in the picture below. Apart from that, there will be similar test structures on the wafer like for IET and HPK (4). Additionally, there are many edgeless test structures (5) with an area of 1.5 X 1.5 cm^2 and conventional baby detectors (6) with 1 X 1 cm^2 around and with DC, Punch-Through and FOCFET biasing. The baby detectors have in total 24 different designs where the active edge and dicing distances have been varied. The wafer design is finished and the processing at VTT has been delayed due to the lack of the resources. The current plan is to finish it by the end of March 2008.



MAIN DETECTOR, 5 X 5 SQCM (1)
MEDIPIX2, 1.5 X 1.5 cm^2 (2)
ALIGNMENT MARKS, 1 X 1 cm^2(3)
HALF MOON TEST STRUCTURE (4)
EDGELESS TEST STRUCTURES,
1.5 X 1.5 cm^2 (5)
BABY DETECTORS, 1 X 1 cm^2 (6)

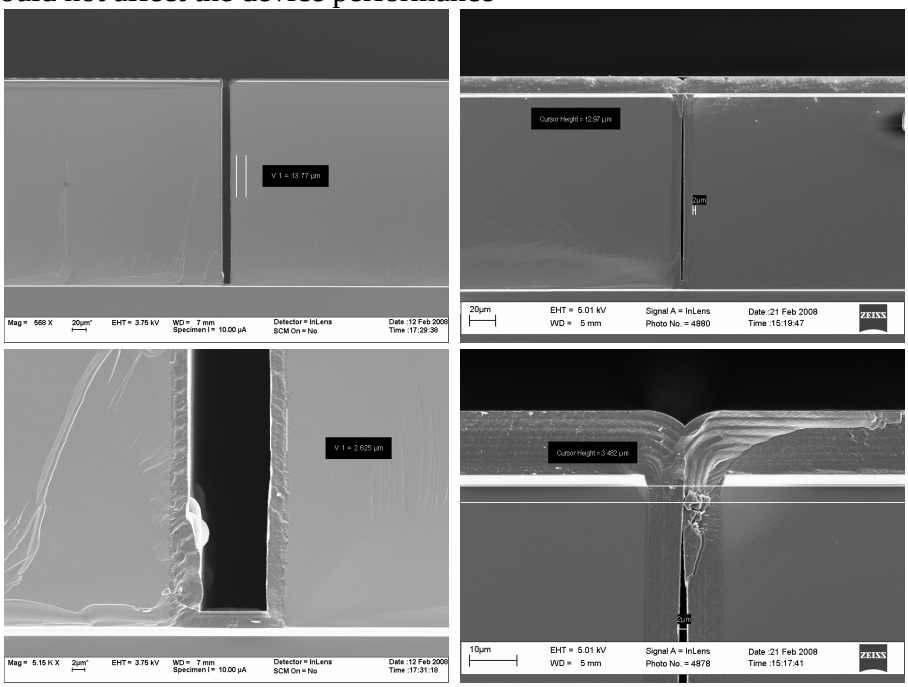
The Planar-3D detectors are being developed with Helsinki Institute of Physics. The design and fabrication is done on 6“(150 mm) wafers at VTT. The first prototype run is on its way and is scheduled to finish 03/08. The fabricated 3D Planar detectors have thicknesses of 150 and 300 µm. The parameters of the microstrip layout were decided together with the associate member HEPHY in Vienna.

The critical process steps at the planar-3D detectors fabrication have been the ICP-etching of the trenches and the phosphorus doped polysilicon filling of the trenches to form the active edges. These so called 3D process steps were very slow and needed a lot of tuning. Now, the steps have been completed (ignoring the ICP-etch chips dicing). The photographs here below show the cross section SEM photographs from the ICP etching process. The process is now tuned to give a smooth stop of the etch to the bonding oxide layer.



Top two photographs: ICP etched trenches into 150 and 300 µm thick high resistive silicon bulk, which are bonded to the support wafers; (bottom) bottom and top of the etched trenches.

The two photographs here below show the poly silicon filling process of the trenches. The bonding and etch mask oxide layers are clearly visible in the photographs. The void inside the poly silicon should not affect the device performance



On the photographs on the left: filling of the trench after 3 μm of poly silicon growth and zoom to the bottom of the trench; (right) completely poly silicon filled trench and zoom to the top of the trench on the bottom photographs.

This work is reported in details in [11]. The produced detectors will be characterized at the Lab test bench and if proven to work at the test beam later.

[11] Juha J. Kallopouska at al., *Silicon Radiation Detector Development at VTT*, in IEEE-Nuclear Science Symposium Conference Record, Honolulu (Hawai), Oct 27-Nov4, 2007; and in http://www.silc.to.infn.it/doc/papers/simo_eranen.pdf, Sixth SiLC Meeting, Dec 2007,

I-2-3: Pixels

The SiLC collaboration is also interested in studying the use of pixel-like sensors in regions other than those covered by the vertex detector. A number of institutes in the collaboration are already involved in R&D activities on pixel technologies. At the moment the activities are focused on CMOS MAPS, DEPFETs, APDs and 3D pixel detectors. Particular attention is paid on connectivity issues, of overriding importance in these technologies.

Pixel detectors could be used in regions needing a spatial resolution finer than that provided by strip detectors or regions in which a smooth transition between pixels and strips is needed to properly resolve ambiguities.

The reasoning for pixel use in tracker region can be found in the simulation section in Ref. [3]

R&D on pixel sensors is not within SiLC main mission, but several SiLC groups pursue research in the field of pixel detector development and mediate communication between SiLC and key groups developing pixel technologies.

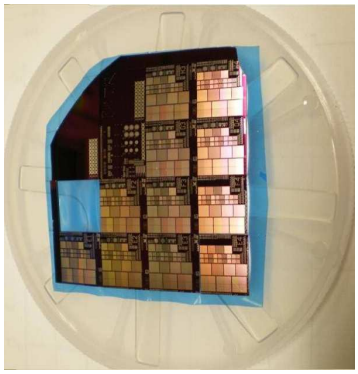
These groups also work on the ways how to implement the pixel technologies into the tracker (optimal detecting element sizes, module shape, readout, etc.)

CMOS APS and APD

Several versions of CMOS APS are proposed for the ILC vertex. Their possible use in tracker is under studies namely at University of Barcelona and Valencia.

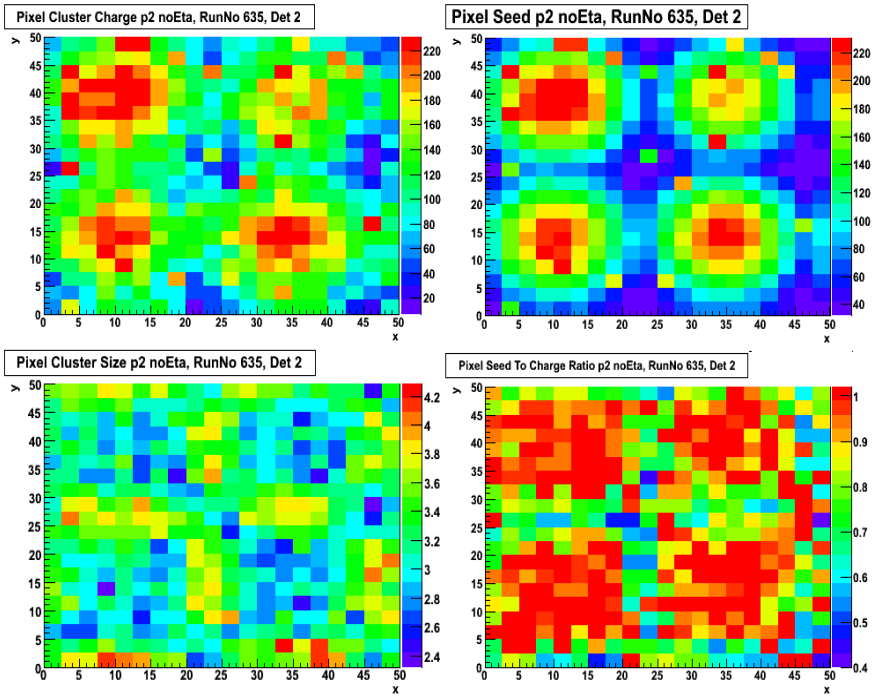
In addition to the standard active pixels novel avalanche pixels with internal amplification can be quite attractive. Due to their high intrinsic gain they can be made very thin and still provide sufficient signal. They are produced out of low-resistivity silicon (which brings easy integration with electronics) in a standard CMOS technology.

The groups active in this development are the Obninsk State University and the University of Barcelona. The photograph here on the right front shows newly obtained prototypes pf pixel APDs



DEPFET: Depleted Field effect transistor (DEPFET) uses active pixels in high resistivity (depleted) silicon. Recent test beam measurement have proven its excellent spatial resolution (better than 2 microns), linked to an impressive signal-to-noise ratio, both achieved at low power consumption. DEPFET collaboration works on the electronic readout development, and module concept for ILC vertex.

Two SiLC groups, IFIC-Valencia and Charles Univerity in Prague are active in the DEPFET development. Both groups have the DEPFET test setups installed and measure detecting performance (noise, charge collection homogeneity, etc.) using laser and radioactive source. The plots here below show results of laser scan: response vs. laser hit position [13].



Laser scan on DEPFET prototypes

The interest on the pixel detectors has been advertised since the start of the SiLC R&D collaboration [1,3]. Up to now the effort was pursued by some teams in SiLC that joined the corresponding pixel R&D collaborations, principaly the DEPFET R&D led by MPI-Munich.
The SiLC collaboration is now launching an R&D effort on 3D-technology and its applications not only on pixels and microstrips (3D-Planar) but also on the 3D vertical integration of the electronics, in cooperation with the worldwide effort in this domain.

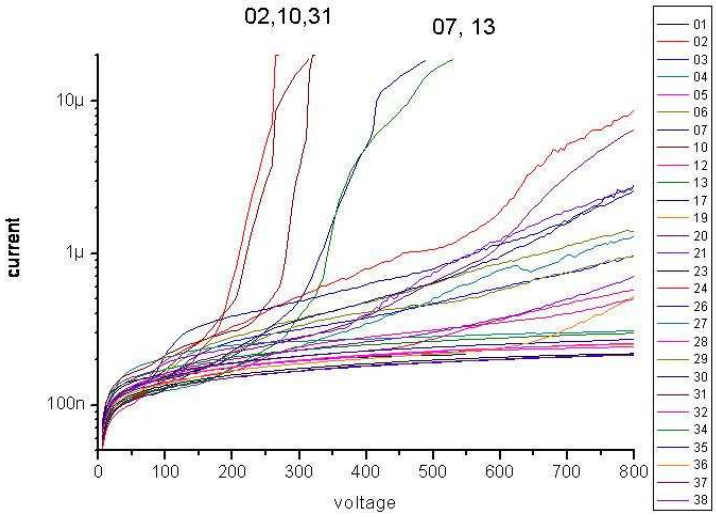
[12] V Saveliev, *Low Material Budget Pixel Detector with High Intrinsic Gain*, http://www.silc.to.infn.it/doc/papers/valeri_saveliev.pdf, presented at the Sixth SiLC Meeting in Torino, Italy, Dec. 2007.

D. Gascon, *R&D on pixel sensors for the Forward tracking for the ILC*, http://www.silc.to.infn.it/doc/papers/david_gascon.pdf , presented at the Sixth SiLC Meeting in Torino, Italy, Dec. 2007.

[13] M. Vos, *DEPFET ILC VTC*, presentation at the TILC08 Workshop, Sendai, Japon, in http://ilcagenda.linearcollider.org/conferenceOtherViews.py?view=standard&confId=2432

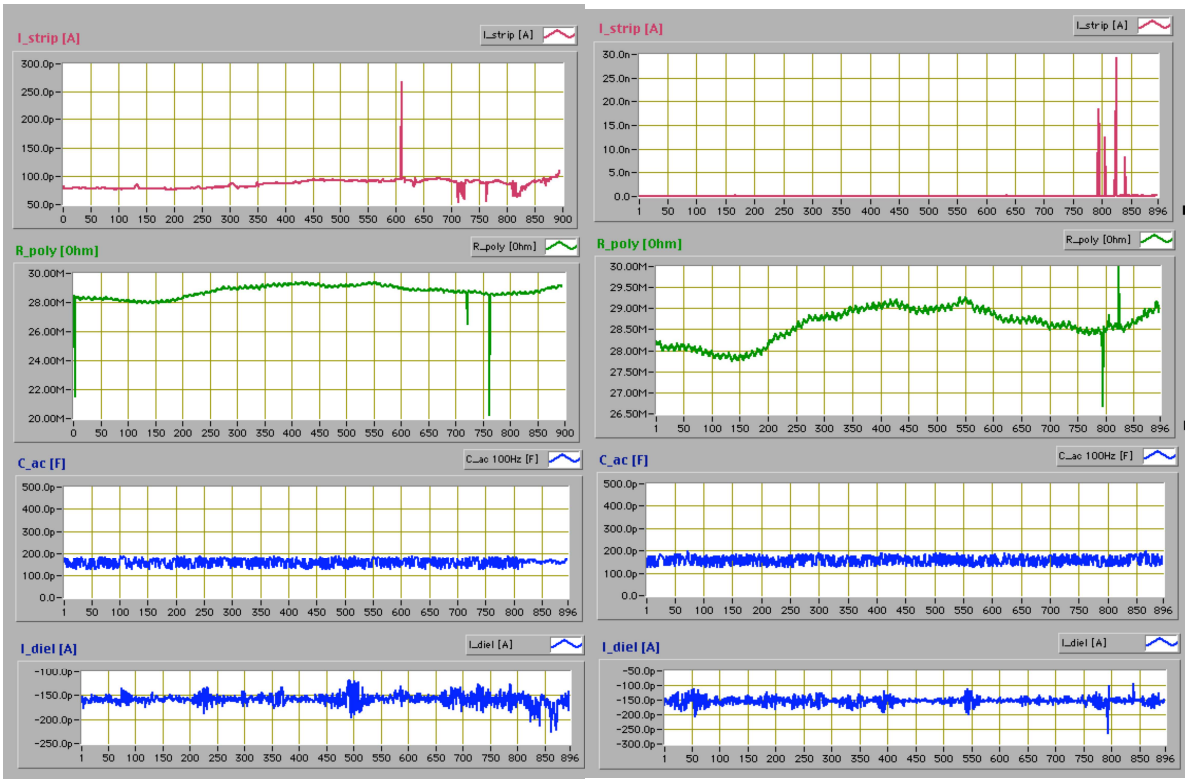
I-2-4: Characterization and Quality Test Control framework

The Quality Control system developed both at HEPHY Vienna and at IEKP Karlsruhe for the CMS experiment [3] was used by both Institutes to test the HPK new microstrip sensors received in October 2007 (see results reported in [10]).
A total of 28 out of the 30 HPK sensors have been tested for IV and CV at Vienna. Ten of them were shipped to Karlsruhe for repeating there these tests. As an example here below is given the IV plot results; all the detectors but 5 were submitted successfully up to 800 V, two went up to 400V and three of them did not sustain more than 250V. Note however that the nominal voltage value for these detectors is around 100V.



IV curves for the 28 HPK sensors tested on the Quality Control test bench at Vienna

Two sensors were submitted to a full strip scan, one in Vienna and the other one in Karlsruhe. The strip scan parameters are the strip leakage, the poly-silicon resistor the coupling capacitance and the dielectric current. The results for the strip scan, on each of these 4 parameters, are shown here below on the even strips (left plots)and the odd strips (right plots).



Strip scan of one HPK sensor, on the left the even strips on the right the odd strips

The strip scan results are identical between Karlsruhe and Vienna the strip leakage is found to be 137 pAmp., the poly-silicon resistor is 28,65 MOhm, the coupling capacitance is 156 pF and the dielectric current is less than 160 pAmp. The interstrip capacitance is 0.94 pF as compared to 0.84pF in the case of the large CMS HPK sensors. The new HPK sensors are essentially of the same level of quality than the one produced by HPK Photonics for CMS; it thus sets the high quality level of these new sensors.
Coming soon are the quality control results from the tests that will be performed on the new structures and the 5 sensors especially treated for the alignment.

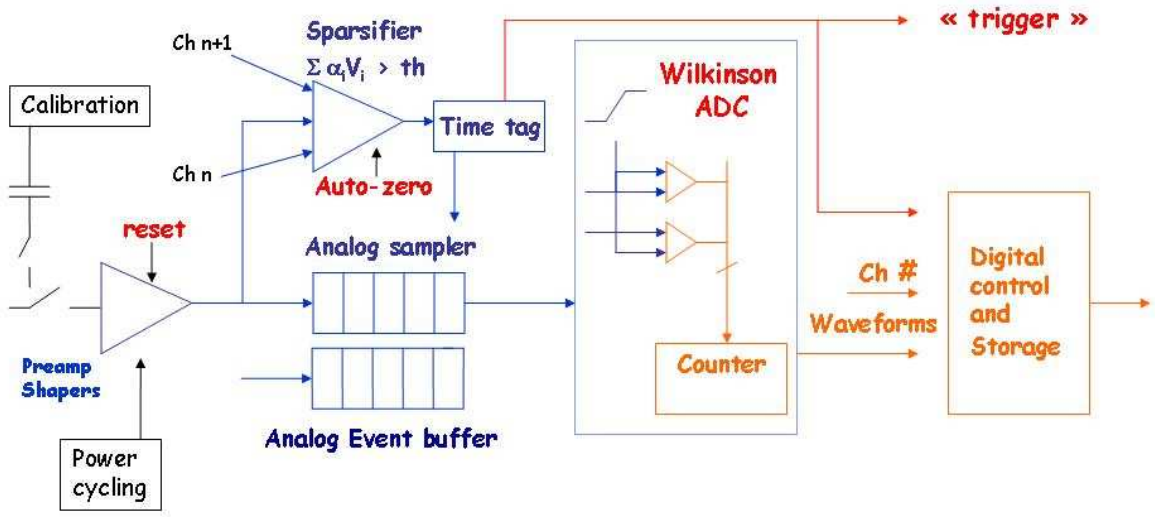
I-3: Electronics R&D

In any detector concept foreseen at the ILC, a front-end readout system for tracking Silicon detectors has to manage millions of channels. Consequently, the amount of material and power per channel has to be carefully optimised keeping noise and readout speed within the constraints of the experiment. It is therefore essential to look for the best integrated technologies available that allow minimizing the amount of material added to the detector, such as connexion capacitances in terms of connectors, hybrid circuits, kaptons, and lead as well to a manageable amount of dissipated power. These technologies allow also implementing efficient data extraction and signal processing techniques such as analogue sampling and on-chip digitisation.. As examples, 180nm and 130nm CMOS readout prototype chips have been designed and tested, and gave satisfactory results in terms of noise and power. Two FE readout philosophies are developed by the SiLC collaboration that are progressing in parallel.

I-3-1 R&D on Time-Over-Threshold Readout (the LSTFE Chip)
The results obtained so far can be found in Ref [3]. A new chip is currently under development in 180 nm CMOS technology.along the same lines than the one developed in CMOS 0.25µm with the promising results shown in [3].

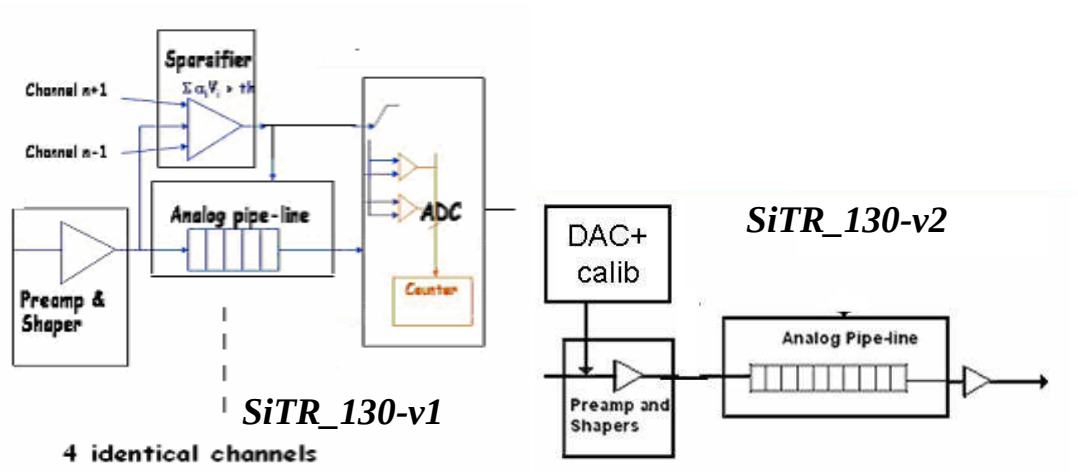
I-3-2 R&D on Deep Sub Micron circuit Front End and readout chip: SiTR_130

Since end 2004, the LPNHE team has launched an active R&D on a FEE readout chip made in DSM (Deep Sub Micron) CMOS technology. The complete schematic architecture of this chip is shown here below.



At the end of 2006, two prototyped versions of this readout chain were coming back from foundry. The year 2007 has been devoted to the full characterization of this new chip. Since end of 2007, the design and construction of a new and even more complete version of this chip in 130nm CMOS technology is under development.

The first of these two prototypes included the FE and readout chain as shown here below (left schema) with 4 such channels per chip. It is labelled as SiTR_130-v1.

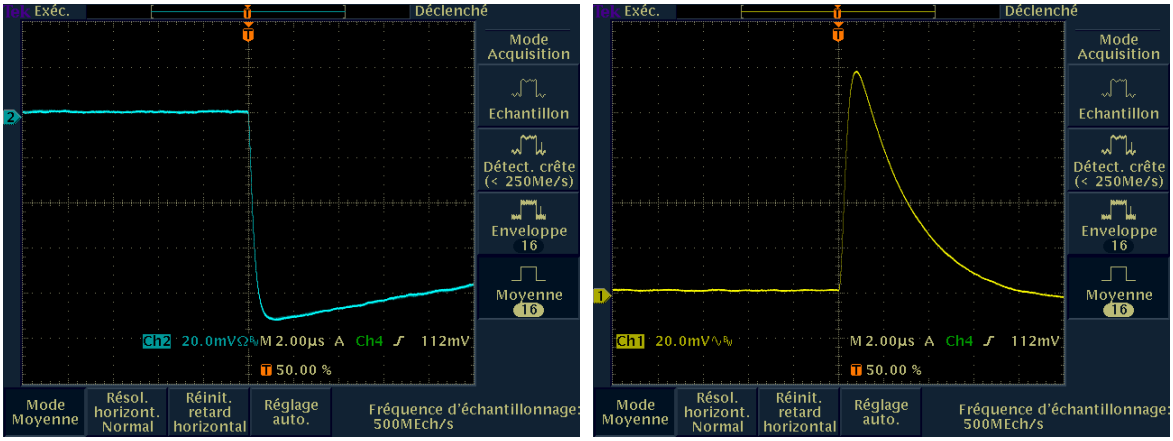


First 130nm prototype chip architecture (left); modified version of the analogue part with an improved pipeline design and an integrated test pulse calibration (right)

A second version, SiTR_130-v2, was developed with one channel comprising only the analogue part with an improved version of the pipeline and a test pulse calibration.

The first prototype was fully characterized in 2007. The second prototype is being tested.

The main results obtained so far are briefly reported here below and can be found in [14].

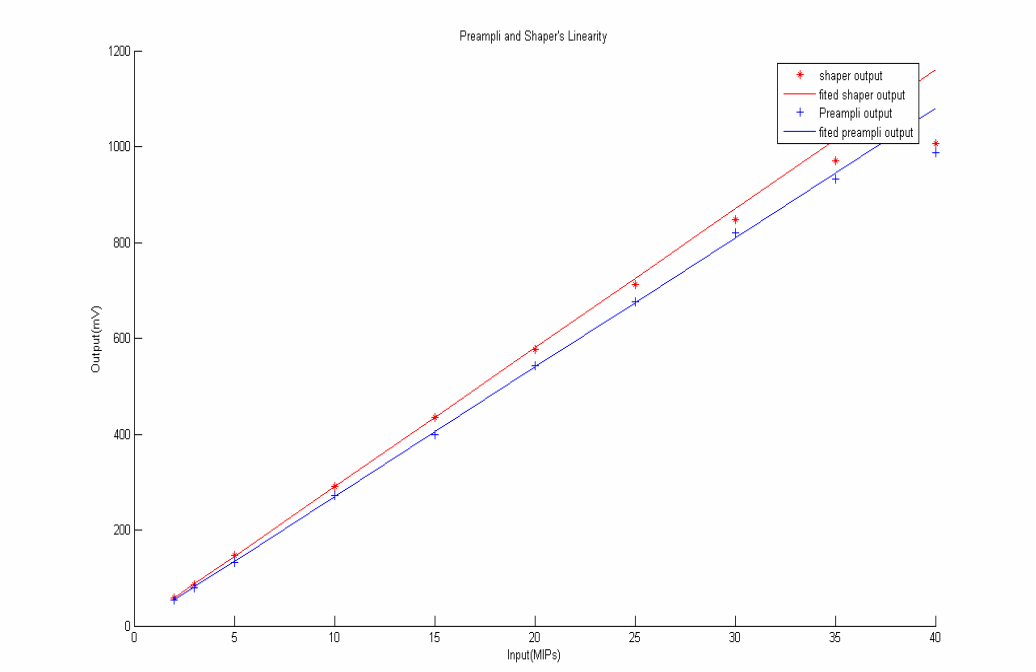


Left pulse height gives the preamplifier signal output; right pulse height is the shaper output.

The peaking time is between 0.8 to 2 µs, for 0.5 to 3 µs expected.

The measured gain is 29mV/MIP; the dynamic range is of 20 MIPs with linearity at 1% and up to 30 MIPs with linearity at 5% (see plot here below)

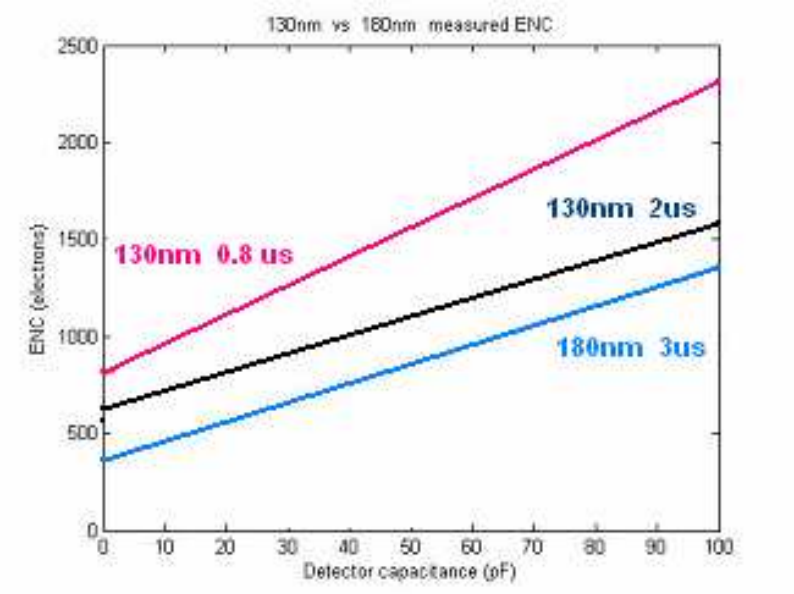
The measured power dissipation for the preamplifier plus shaper is measured to be 245 µWatt in CMOS 130nm technology, slightly higher than in the previous version in 180nm CMOS technology.



Linearity curve of the preamplifier (blue curve) and the shaper (red curve) with measured points and fitted linearity curves.

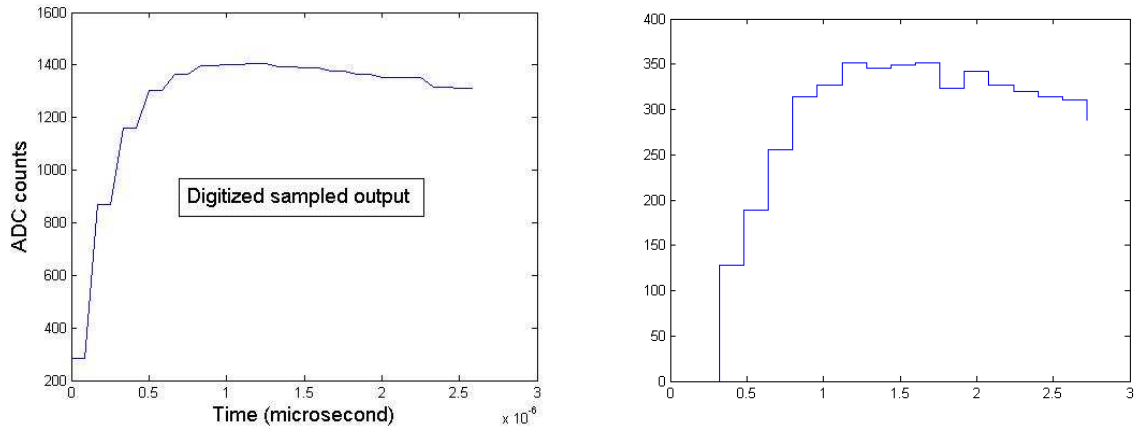
The noise performances are measured to be of 850 e- + 14 e-/pF with a peaking time of 0.8µS and of 625 e- + 9 e-/pF for a peaking time of 2µs. It has to be compared with the measured noise with the prototype in 180nm CMOS technology from UMC for which the measured noise was given by 375e- + 10.5 e-/pF.

Thus, contrary to the very pessimistic results given by the simulation, the results are rather comparable to those obtained with the previous prototype made in 180nm technology as shown in the plot here below. Indeed the simulation was predicting a factor 4 to 5 higher noise when going from 180 to 130nm CMOS UMC technology.



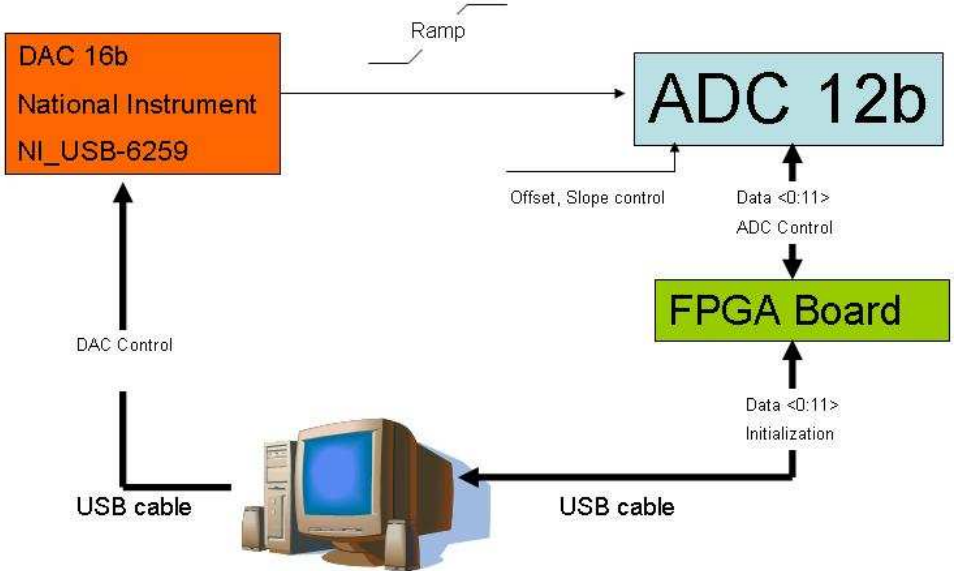
Measured ENC noise as a function of the detector capacitance and of the peaking time

The 16-cells pipeline was tested as well with a sampling rate of 12 MHz and a readout rate of 10 KHz, both with a calibration test pulse (see the digitized output of the signal on the left plot here below) and with a laser diode exciting a Silicon module read out by the chip (see the shape of the signal as delivered at the digitized output of the chip on the right plot here below).



Measured digitized output of the pipeline for a test pulse (left) and for a laser diode signal exciting a Silicon detector read out by the new chip (right).

Finally the ADC block was also tested and characterized with the test set-up shown in the schematic view here below. As a result an effective number of bits of at least 9,7 for 12 expected was determined in the worst case.



Schematic view of the test set-up for characterizing the ADC block in the SiTR_130-v1 chip.

After characterizing each block of the SiTR_130-v1 chip and thus the full functionality of this device, it was connected to one of the Silicon modules and tested in real conditions at the test beam at CERN (see Section II-2)

[14] EUDET-Memo-2007-29, *Silicon Strips Detectors Readout Chip in Deep Sub-Micron CMOS Technology* in http://www.eudet.org/e26/e28/e182/e516/eudet-memo-2007-29.pdf by J-F Genat, T-H.Pham, A. Savoy-Navarro.

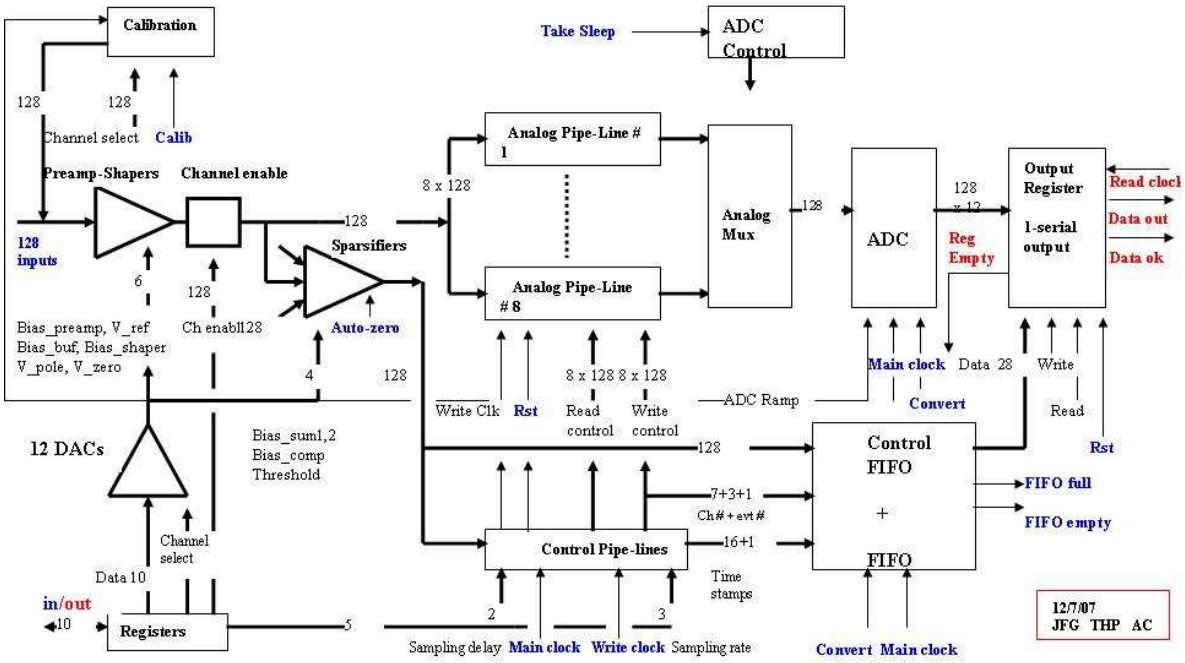
A. Comerma et al., *A 130nm CMOS evaluation digitizer chip for Silicon strips readout at the ILC,* in Proceedings of the TWEPP (Topical Worshop on Electronics for Particle Physics), at Prague, Sept 3-7, 2007 and of IEEE-Nuclear Science Symposium, held in Honolulu (Hawai), Oct 28-Nov 4, 2007.

I-3-3 Towards the new SiTR_130-96 chip to equip the Silicon detector prototypes

Based on the successful results obtained with the SiTR_130-v1 prototyped chip, a new version of the FE readout device is being designed starting end of 2007. The detailed schematic architecture of this new chip is shown here below.
The size of one block in the multi-project foundry is of 5x5mm^2; it allows locating a total of 96+1 channels, instead of the 128 originally foreseen as still in the detailed architecture schema here below. Each channel include the complete readout chain schematized here below. It is built with the 130nm CMOS UMC technology as the previous version with 4 channels and it will include an improved VFE in terms of signal shape, an 8x8 deep pipeline , the chip digital control, digital buffer, processing for test pulse calibrations now part of the chip (it was included in the FE board in the previous version), sparsification and power cycling.

A special care is given to testability; an additional channel, channel 97 will provide a direct access to each of the main blocks of the chip architecture, allowing for a test of each of this

piece independently. A mixed mode simulation is developed for the first time that will allow simulating and thus testing the full functioning of the device before sending it to the foundry. It is expected to be sent to foundry on April 15. It is labelled as SiTR_130-96.



Detailed architecture of the new SiTR_130-96 chip

Even if this foundry is successful, it is foreseen to send a new foundry by the end of 2008 or beginning 200, with some updates on the present version according to the results obtained when characterizing these new chips. Furthermore, the goal is to produce possibly still before end of 2009, a new version of the chip with a higher multiplexing in channel (i.e. at least 256 channels per chip) and if available using the 90nm CMOS technology,
These new options will be in any case experienced if not in 2009, the year after. Finally, the 3D vertical integration of the electronic is also among the future goals (see next).

I-3-4: Wiring on detector and cabling

Developing the inline pitch or direct wiring of the chip onto the detector has started this last year as part of the SiLC R&D project. This proceeds in several steps and in collaboration with Industry.
The first step in progress consists in bump bonding the chip onto the microstrip sensor as usually done with the pixel devices but not yet performed with strips.
The first attempt is based on using on one hand the new HPK sensors with 50 µm readout pitch and to experience bump bonding the new SiTR_130-96 chip onto the sensor.
A NdA contract has been signed between CNRS-IN2P3 and HPK Photonics to develop this technique using both devices. HPK will provide the sensor and expertise in bump bonding and LPNHE will provide the chip and the needed test set-up for comparing the performances of the chip when bump bonded to the sensor or when connected through an hybrid board.
This is a long term process as it needs to have the chip produced and fully tested and the bump bonding technique well in hand to produce the first demonstrator. It is hoped to have such a demonstrator by the end of 2008, if the foundry in April is successful and if no problem on the HPK side too. The test procedure will then last over about 6 months in 2009,

before having in case of success, the first prototypes installed on detector prototypes in a test beam. This would not occur before fall 2009 in the most optimistic scenario.
For the longer term the 3D vertical integration technology is starting to be investigated.

Part II: The R&D Tools

A lot of work has be performed with real advances over this last year on the development of the tools needed for achieving the challenging R&D goals [15]. The main tools are indeed simulations tools and test set-ups both at the Labs and at test beam facilities.
A coordinated effort has been launched, led by V. Saveliev (OSU) and M. Vos (IFIC). It presently gathers people from Charles University in Prague, HEPHY in Vienna, IFIC in Valencia, LPNHE in Paris, OSU in DESY, UCSC in Santa Cruz. It is expected t have a reinforced collaboration with the Korean Group as well with a few more people from other teams in SiLC collaboration. The links with the ILC detectors have been established, primarily with the ILD optimization group led by M. Thomson in the framework of MOKKA. A connection with the 4th concept through ILCROOT is starting to be developed as well.

II-1: Simulations

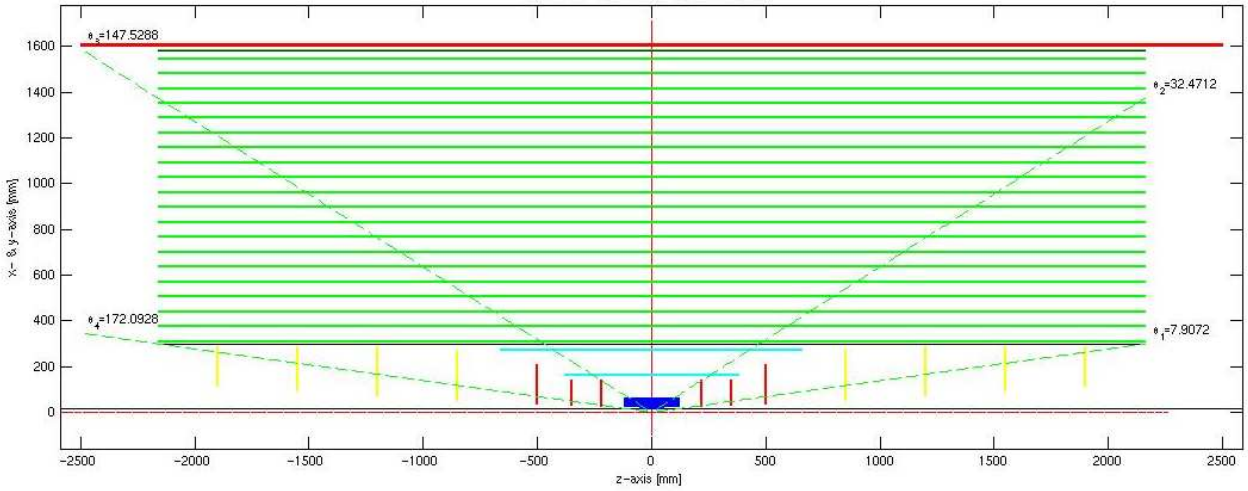
In this phase of the detector design Monte Carlo simulations are an invaluable tool. Detector design parameters must be chosen to maximize the physics output of the experiment. The SiLC collaboration has therefore invested considerable effort in the development of tools for Monte Carlo studies. Much progress has been made to establish the dependence of the track parameter resolution (in particular the momentum resolution) on the layout and material of the tracker through *fast simulation*. Maybe even more importantly, the last year has witnessed the transition to *full simulation*. Much attention has been devoted to the development of the software that will allow detailed GEANT4 simulations of the detector response, a digitization package to transform the energy deposition in a realistic signal (including noise etc.) and the reconstruction software.
In this section, the most important developments are briefly presented, as well as some results from the first studies.

II-1-1 Simulation tools I – fast simulation

In the "*fast*" approach to detector simulation the trajectory of the particle in the detector is simulated using a simple model (typically a helix). The position measurements on the detectors are simulated by smearing the crossing point of the particle and a simple detector geometry (see Figure here below) by the expected detector resolution. The resolution of the five track parameters is then established by a track fit through these points.

Since it was formed, the SiLC collaboration has played an important role in the development of *fast simulation* tools that allow to study the resolution for charged tracks in a simplified geometry. Two of the key packages used for the early design optimizations of the detector concepts – SGV[16] and LCDTRK[17] - were developed by members of the collaboration. As these packages are well-established since several years and have been presented in great detail in previous reviews[3] a description of these packages is beyond the scope of this document.
In recent years a third package, the LiCToy[18], has been developed by HEPHY in Vienna. The algorithms used in the tool – in particular the Kalman filter track fit including material effects – represent the state of the art in high energy physics experiments. The user-friendly GUI allows the use of this tool even by non-experts.
The detector model corresponds to a generic collider experiment with a solenoid magnet, and is rotational symmetric w.r.t. the beam axis; the geometric surfaces are either cylinders

("barrel region") or planes ("forward/backward region"). The magnetic field is homogeneous and parallel to the beam axis, thus suggesting a helix track model. Material causing multiple scattering is assumed to be concentrated within thin layers.



Simple detector geometry describing the LDC tracker in LiCToy similar to the one in SGV

The mini simulation generates a charged track from a primary vertex along the beam axis, performs exact helix tracking in a homogeneous magnetic field with inclusion of multiple scattering, and simulates detector measurements including inefficiencies and errors. The basic version supports Si strip detectors (single or double sided, with any stereo angle), pixel detectors and a TPC; systematic and/or stochastic inefficiencies; and uniform or Gaussian measurement errors.

The simulated measurements are then used to reconstruct the track by fitting its 5 parameters and 5x5 covariance matrix at a given reference cylinder, e.g. the inside of the beam tube (they may be converted to a 6-dimensional Cartesian representation). The method used is a Kalman filter, with the linear expansion point being defined by the undisturbed track at that surface. The track fitters that are at the same level of sophistication as the those of running experiments. Importantly, the track fit includes material effects. The quality of the fits is cross-checked by an inspection of the chi-squared and pull distributions.

In the last year, LiCToy has established itself in the SiLC collaboration as a reliable and flexible tool. The results on a series of test setups have been verified against other fast simulation packages.

The fast simulation approach described however implies three important limitations. The simulation of tracks and hits as ideal helices represent ideal tracks that do not suffer nuclear interactions, do not loose energy through the emission of bremsstrahlung, etc. The smearing of hits with a Gaussian (or uniform) distribution ignores the tails of the hit resolution (i.e. due to the emission of delta-electrons). The third, and maybe most important, limitation comes from the fact that single particles are simulated. This implicitly assumes the track finding (pattern recognition) phase converged successfully; the effect of overlapping hits and the difficulties that arise in the assignment of hits to tracks are not addressed by fast simulation.

II-1-2 Simulation tools II – Full simulation framework of the ILC Spectrometer

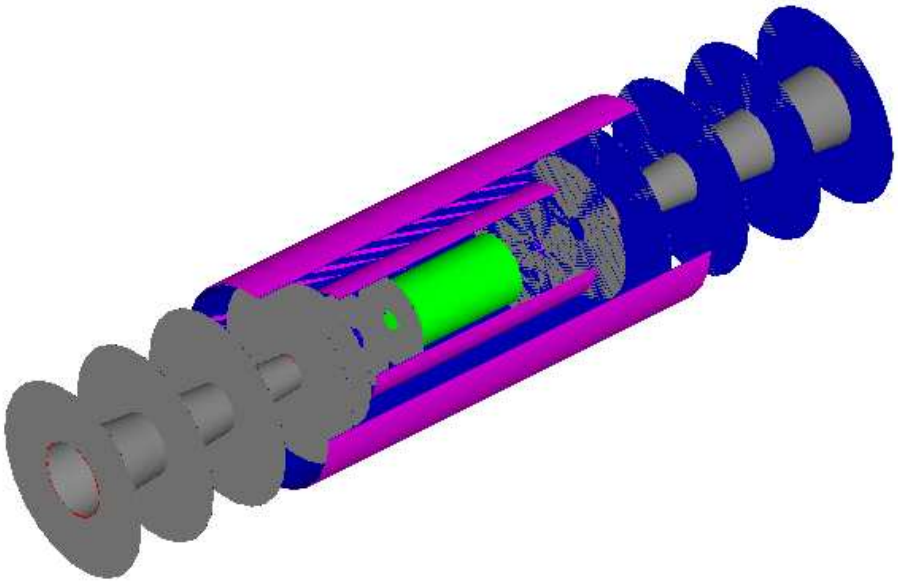
To study all aspects of the detector performance full simulation is needed of the interactions of all particles in the event (including backgrounds) with a detailed model of the detector. The full Monte Carlo simulation of the sub-detector components is as well a powerful tool for the *optimization* of the overall ILC spectrometer as well as of each of its components..

The SiLC collaboration proposed and studied the ensemble of Silicon tracking components that surrounds the TPC central tracker in the LDC concept, as described in the LDC DOD.
The SiLC collaboration is responsible for the definition and study, in the full simulation framework MOKKA of ILC, based on Geant4 simulation tool, of the silicon tracker elements in the model of the International Large Detector (ILD), namely:

- *the Silicon Intermediate Tracker* (SIT) that covers the central and innermost part of the tracking volume, between the vertex detector and the Time Projection Chamber (TPC).
- *The Forward Tracking Disks* (FTD) that provide coverage for charged tracks in a polar angle range from 6 to 30 degrees.
- *The Silicon External Tracker* (SET) that provides precise space points at large radius. This detector is to be installed between the outer envelope of the TPC barrel and the face of the electromagnetic calorimeter (ECAL).
- *The Endcap Tracker Disks* (ETD) that fulfil a similar role in the forward region. This detector is to be installed between the TPC end-plate and the ECAL end cap.

All these four Silicon components are now implemented in the simulation framework MOKKA, as basic components, including possibility of flexible change of the geometry parameters according to the overall design in flight, by implementation of the *super driver codes* of the geometry definitions. The ILD optimization group is finalizing the full ILD detector geometry and is preparing for a mass production of Monte Carlo data for physics and detector optimization studies according to the physics benchmarks. The complete set of four Silicon tracking components are ready for this first round.

The Figure here below shows as, an example, the detector model for the Silicon Intermediate Tracker and the Forward Tracker Disks of the Large Detector Concept.



Detector model for the Silicon Intermediate Tracker and the Forward Tracker Disks of LDC in the MOKKA simulation framework (the green colour component is the VDX).

The SiD tracker geometry has been implemented in MOKKA by the SiLC collaboration and a first step was made to define the silicon tracker elements in one of the scenarios in the 4th concept. It is clear, however, that the effort on these two detector concepts is behind compared to the progress on ILD.

II-1-2-1 Simulation tools III – digitization

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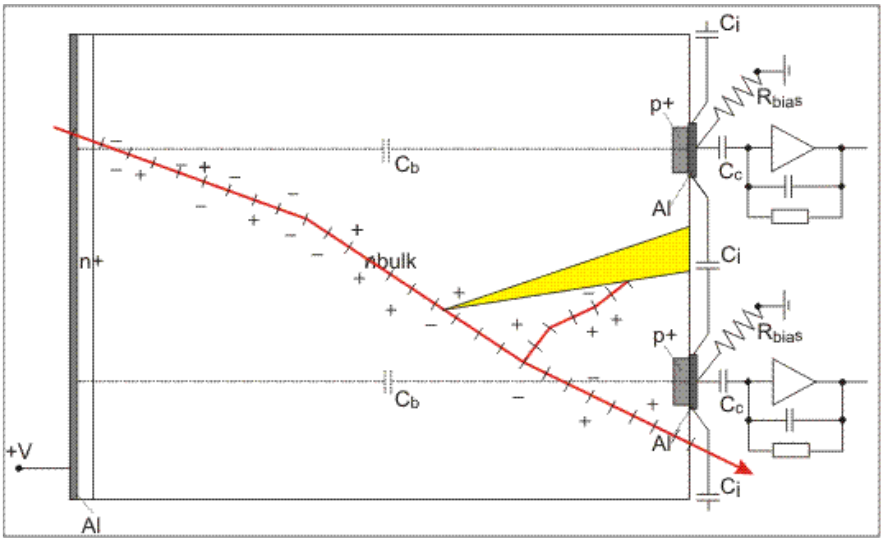
The full MOKKA simulation, based on Geant4 and described in detail in the previous section gives as output all information about particles in each event, including spatial information, where the particle crossed the detector, and its deposited energy. The conversion process of deposited energy into a realistic detector signal is called digitization and is performed by the digitization package. Such a package, called SiStripDigi and based on a detailed physical model of charge collection in micro-strip detectors is being developed within the ILC simulation framework, namely Marlin, by Charles University in Prague.
Its aim is twofold: on the one hand it will provide a detailed detector model that is crucial to understand test-beam results on prototypes on the other hand it provides a reference to the much simpler model used in the full simulation.
The detailed model includes following physical processes: charge carriers drift, diffusion, Lorentz shift in magnetic field and so called etha correction, respectively mutual strip crosstalk (dependent on AC or DC coupling of individual sensors). As physical parameters one just defines: detector bias voltage, detector depletion voltage, the sensor temperature and as precision parameters, connected with numerical methods used: absolute spatial precision and relative angle precision. Due to a fact, that the package is completely integrated into ILC simulation framework, geometry information is simply read from the GEAR xml file and doesn't have to be defined by a user. As the package represents more complex solution than usually required, it's aim is twofold: on one hand it should provide a detailed detector model that is crucial, when one wants to understand the test beam results measured on detector prototypes, on the other hand, it will hopefully provide a reference to much simpler models usually used in full simulation.



II-1-2-2 Simulation tools IV – reconstruction

To study the tracking performance within the MarlinReco framework, a Kalman filter track fitter has been implemented in object-oriented C++ code. It is based on the CMS track

reconstruction software[19][1]. The tool-kit comprises a sophisticated track propagation model - containing the deviation of the charged particle trajectory by magnetic fields of arbitrarty complexity. The interaction with thin layers - multiple scattering and energy loss - are taken into account by the propagator. Given a trajectory state (a set of measurements fully describing the particle parameters and their errors) a new trajectory state with correctly transformed errors can be predicted on any detector plane. Tracker hits are represented as 2D measurements on a plane. If a compatible hit is found on the plane, the hit may be added to the track. The trajectory state is updated to take into account the newly added information through the Kalman Filter formalism.
The original code has been thoroughly validated against large Monte Carlo samples by the CMS collaboration. The interface to the LCIO format of the hits and to the detector geometry in GEAR has been tested thoroughly. Internal consistency is cross-checked by the Monte Carlo pull distributions. The results are furthermore tested against several fast simulation tools. Predictions for the resolution of all track parameters on a variety of toy models have been compared to LiCToy, LCDTRK and SGV.
To derive reliable constraints on the detector design from pattern recognition a state-of-the-art track finder has furthermore been implemented in MarlinReco. A simple, but extremely powerful algorithm is employed. The combinatorial algorithm is one of the most popular approaches on the market: it is the baseline pattern recognition algorithm of both ATLAS and CMS. Currently, the implementation is limited to only one detector region: the forward tracking disks.
Throughout the pattern recognition process, propagation (extrapolation) and updating of trajectory descriptions are done using the tools provided by the Kalman filter kit described before. Thus, at all stages the fit to the trajectory (and its errors) yields an optimal estimate given the available information.
The combinatorial track finder starts off with a collection of seeds. Typically, hit pairs plus beam constraint or triplets in high-granularity, low-occupancy detectors are chosen. For each seed the weakly constrained track model is extrapolated to the following layer. In this layer, compatible hits are searched for. For each compatible hit, a copy of the track candidate is made and updated with the hit information. All candidates are in turn propagated to the next layer, where the process is repeated. The iterations for a given candidate are only stopped if no more compatible hits are found (in actual implementations the stopping conditions are more complex to deal with layer inefficiencies).

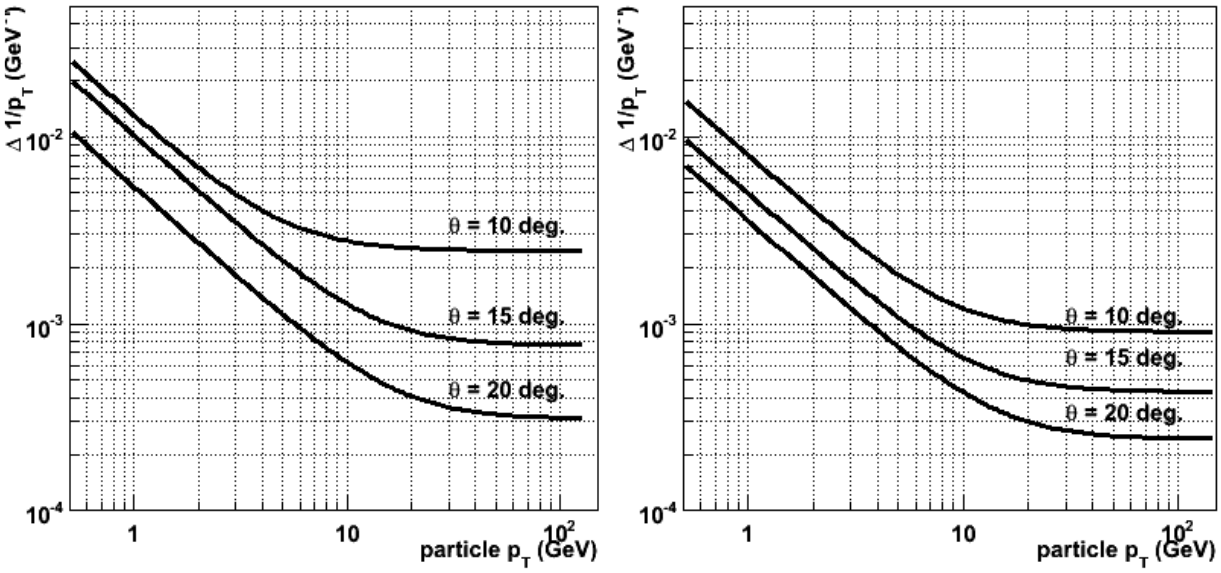
II-1-3-1 Results – resolution

The resolution of different tracker layouts has been studied in great detail. In particular, the differences between the performance of a tracker based on an all-silicon layout and a mixed gas plus silicon detector has been discussed extensively. Without pretending to do justice to the large effort by many people, in this section a recent study is briefly presented.

In the past, much of the discussion has concentrated on the central tracker. The forward region has traditionally received less attention. The transverse momentum resolution in the forward region is degraded significantly by the unfavourable orientation of the solenoidal magnetic field. In the two figures here below the transverse momentum resolution is shown for two detectors based on the LDC FTD layout that differ in the material budget and the resolution of the RΦ measurements. The detector of the leftmost figure – with approximately 1 % of a radiation length per disk and a spatial resolution of 10µm - is one that could be built with proven technologies. The second detector represents a severe challenge: the material of the

1 The author acknowledges the collective effort of the CMS collaboration in the development of this software

innermost disks is reduced by a factor 10, that of the outermost disks by a factor 2, while the spatial resolution is improved by a factor 2 throughout.



Transverse momentum resolution versus transverse momentum. Challenging detector: 10µm RΦ resolution, 1.2 % X_0 / disk in the Three innermost disks, 0.8 % X_0 / disk in the remaining four. LDC "Tesla" FTD layout.

Transverse momentum resolution versus transverse momentum. Challenging detector: 5µm RΦ resolution, 0.1 % X_0 / disk in the three innermost disks, 0.4 % X_0 / disk in the remaining four. LDC "Tesla" FTD layout.

Clearly, the momentum resolution is improved dramatically by these changes of the detector specifications; the momentum resolution at all angles is improved by a factor two. LiCToy studies confirm that another factor of two in the asymptotic resolution at high p_T can be gained by extending the lever arm of the Forward Tracking Disks. More recent versions of the LDC FTD indeed cover the full length of the TPC. It must be noted, however, that the performance remains far from the several times 10^{-5} considered for the central tracker.

II-1-3-2 Results – pattern recognition

The pattern recognition of very forward tracks in the LDC is considered particularly challenging. The background due to incoherent pair production off beamstrahlung photons, negligible in much of the tracking volume, contributes significantly to the occupancy[20, 21,22]. Low-momentum tracks of all polar angles curl up to form loopers that leave the detector through the very forward tracker. The coverage of the "long barrel" vertex detector is incomplete; for tracks emitted at a polar angle of less than 12.5 degrees the innermost measurement is provided by the Forward Tracking Disks.
To evaluate the pattern recognition performance, a dense signal topology (top-antitop events) is chosen. The beam-induced background due to a variable number of bunch-crossing is superposed on the signal event. The combinatorial track finding algorithm is applied to the standalone Forward Tracking Disks. For this study, the algorithm is run "inside-out", i.e. starting from seeds created by combining hits in the innermost forward tracking disks and working its way towards the outermost disk.

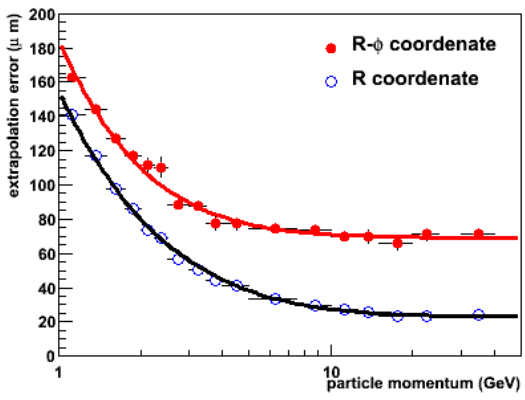
The traditional quality marker for pattern recognition is the channel occupancy. In the table below the peak density of hits in the innermost disks is given for three technology options. To determine the channel occupancy these results must be multiplied by the average cluster size. The contributions from signal and background are given separately in the third column: the peak occupancy in jets in tt-events is found in jets, while for the background the peak occupancy is that of the innermost ring of the tracking disks.

Technology	Cell area (□m x □m)	Integration time	Peak occupancy
□Strip	50 x 10^5	300 ns	5 % + 1 %
Hybrid pixel	50 x 500	300 ns	2 x 10^{-4} + 4 x 10^{-5}
VXD	25 x 25	50 □s	6 x 10^{-6} + 1.5 x 10^{-4}

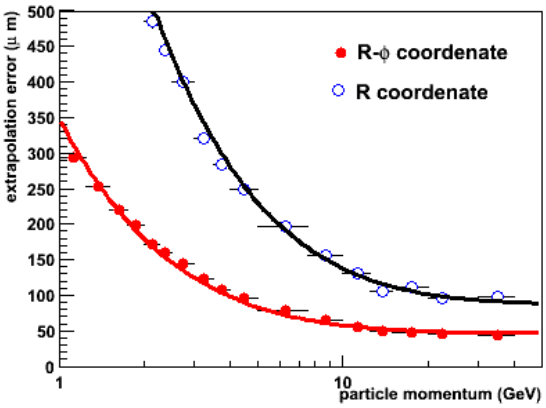
Active sensor area per channel, the integration time and the occupancy for three options of technology: The two terms in the occupancy correspond to the peak occupancy in the signal and the contribution due to the background, respectively.

The occupancy of micro-strip detector reaches 5 % in jets in tt-events. For hybrid pixel detectors – with much reduced cell area - the occupancy is two orders of magnitude lower. The contribution of the beam-induced background to the occupancy is non-negligible, but due to the single bunch-crossing read-out capabilities of these technologies, it remains well below the peak density in the signal topology. The novel pixel detectors developed for the ILC vertex detector allow going to much smaller pixel size. The rolling shutter read-out of these detectors, however, results in a much longer integration (here, the results for an integration time 50 μs are given). Thus, the balance of the contributions to the occupancy is shifted; while excellent occupancy is obtained even in the core of highly energetic jets, the occupancy is now dominated by the background.

Another key ingredient in pattern recognition is the precision with which tracks candidate can be extrapolated on the following layers. All hits that are within several times the extrapolation error will be considered compatible with the track candidate. The probability to pick up spurious hits (i.e. create ambiguities) thus increases with the extrapolation error. As an example, the first three FTD disks are equipped with pixel detectors providing 10 × 10 μm^2 space point resolution, while the four outermost disks have single-sided strips with virtually no R resolution: the space point resolution is simulated by 10 μ m × 3 cm.



Extrapolation precision: a track candidate made up of 3 precise space points in the pixel detector is propagated to the 4th disk.



Extrapolation precision: a track candidate made up of three hits in the pixel disks and two in the silicon micro-strip detector is propagated to the

In the two figures here above the extrapolation errors in the RΦ and R coordinate are given as a function of the transverse momentum of the track. The track fit to the hits in the first three

disks yields a precise prediction of R on the 4th disk (leftmost figure), while the RΦ precision is limited by the uncertainty in the momentum resolution. Addition of more hits yields a much better constrained momentum. Therefore, the extrapolation to the 6th over a much larger distance (20 cm instead of 12 cm) is nearly as precise in RΦ as in the first disk. The R-coordinate, on the other hand, is not measured by disk 4 and 5. Therefore, the error increases at every next disk, reaching several mm for low momentum tracks.
Compared to the vertex detector, where very precise measurement are spaced by distances of few millimeters, the uncertainties on the extrapolated position can be up to two orders of magnitude larger. Therefore, a hit density (number of hits/mm^2) that is quite tolerable in the vertex detector, may lead to irresolvable ambiguities in the forward tracking disks.
The example in the two figures here above shows clearly how the R-segmentation of the detector has a large impact on the extrapolation precision. To determine the optimum value, the track finder was run using a series of different combinations of R-resolution in disks 1-3 and 4-7. The results confirm that there is no gain in reducing the R-resolution below the extrapolation error due to multiple scattering. The performance of two setups with R-resolutions in the first disks of 10 and 100µm is identical. The resolution requirement in the outermost disks is more relaxed. The algorithm is found to converge rapidly for all R-resolutions up to 1 mm. Thus, double sided micro-strip detectors with a small stereo angle would be sufficient. The pattern recognition performance of a detector based on single-sided strips, even in combination with pixel detectors in the innermost disks, is found to be insufficient.
The material budget is found to have a strong impact on the pattern recognition performance. Increase of the material beyond 1 % X_0 / disk leads to a strong degradation.
The integration time of the innermost three disks has also been varied. The combinatorial algorithm is found to converge for a number of integrated bunch crossing of up to 10.

II-1-4 Summary

Monte Carlo simulations are an invaluable tool in this stage of the detector design. Over the last year, the SiLC simulation work package has contributed in a very significant way to the development of tools. The LiCToy has been established as a reliable and user-friendly fast simulation tool. The geometry of the all four silicon tracker elements (i.e. SIT, FTD, ETD and SET) of the Large Detector Concept has been implemented in the MOKKA framework, as well as a detailed model for the digitization of the signals.
The detector studies moreover rely on sophisticated reconstruction software. A standalone track finder has been implemented for the Forward Tracking Disks.
The impact of design variations on the tracker performance has been studied extensively. Recently, the forward region of the tracker has received considerable attention. The transverse momentum resolution at small polar angle is degraded considerably by the unfavorable orientation of the magnetic field. The performance loss should be minimized by a combination of the largest possible lever arm, excellent RΦ resolution and minimal material.
Pattern recognition requirements can have a significant impact on the detector design. In the very forward region, with a considerable level of beam-induced background and an abundance of low momentum tracks, pattern recognition is particularly challenging. The first full simulation studies indicate that a combination of considerable R-segmentation, fast read-out and minimal material is required for efficient and pure track finding.

[15] Presentations by V. Saveliev and M. Vos at the first ILD Meeting, Zeuthen-DESY, Jan 2008.
[16] M. Berggren, SGV simulation, http://delphiwww.cern.ch/~berggren/sgv_ug/sgv_ug.html

[17] B. Schumm, *Tracking at the ILC, why silicon is best and how it can be optimized*, NIM A 579 (2007) http://confluence.slac.stanford.edu/display/ilc/lcdtrk

[18] W. Mitaroff, *the LicToy: a flexible tool for detector optimization*, LCWS07

http://wwwhephy.oeaw.ac.at/p3w/ilc/talks/08_ILD_Zeuthen/Mitaroff_LiC_rev.pdf

[19 W. Adam et al., *Track reconstruction in the CMS tracker*, CERN-CMS-NOTE-2006-041

[20] D. Schulte, PhD. thesis, University of Hamburg 1996.

[21] A. Vogel, *Update on the beam related backgrounds in the LDC detector*, LCWS07

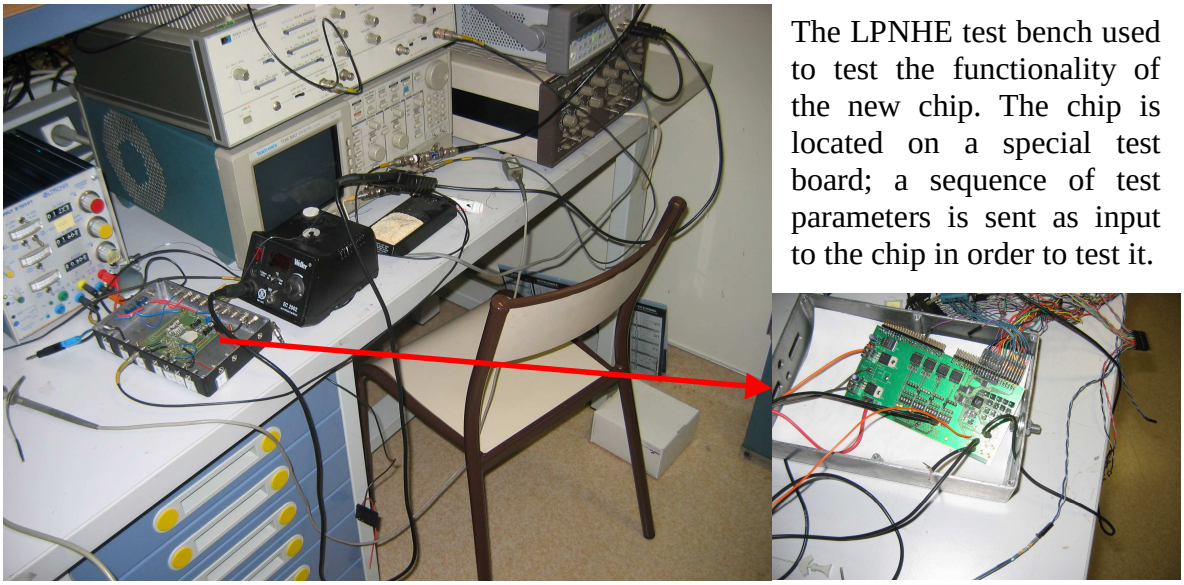
[22] C. Rimbault et al., *Study of incoherent pair generation in Guinea Pig*, EuroTev report 2005-016

II-2: Lab test benches , description and present results

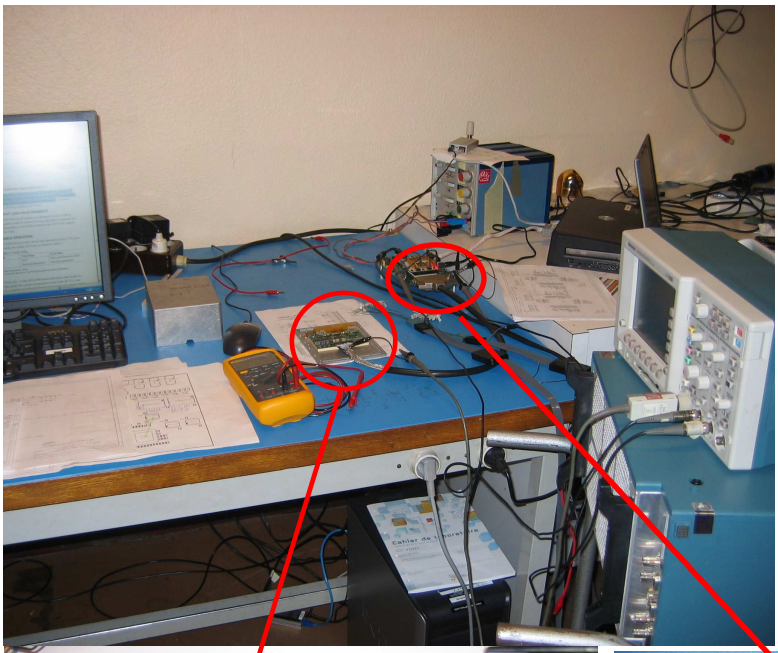
Different Lab test benches are developed, they need continuous upgrade and new ones have been lately developed in the collaboration. Among those, three main types are at disposal: the quality control of the sensors as developed at HEPHY and IEKP and described in [3], the Lab test bench for characterizing the new FE readout chip, the related DAQ system and the new modules at LPNHE also described in [3], that we labelled as ‘’multipurpose Lab test bench’’. Another one similar to this is for example available at UCSC-SCIPP. Finally a new test bench is being set-up at IFCA for developing the alignment hybrid system and related issues.

II-2-1: Multipurpose Lab test bench

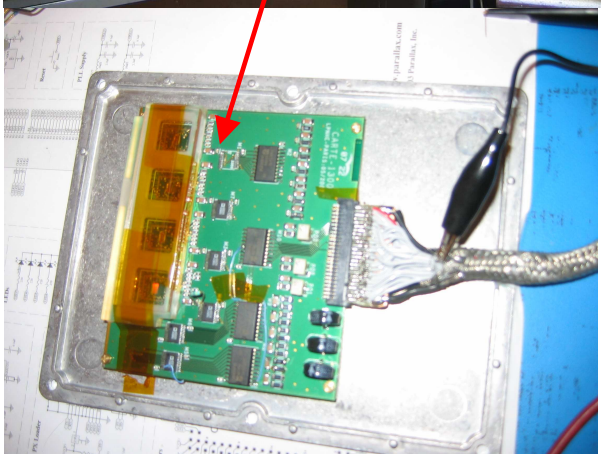
The test bench developed at LPNHE, has been evolving this last year at the same time that the new chip was characterized. The related FE boards that host the chips and the associated new DAQ system were built and tested as well.

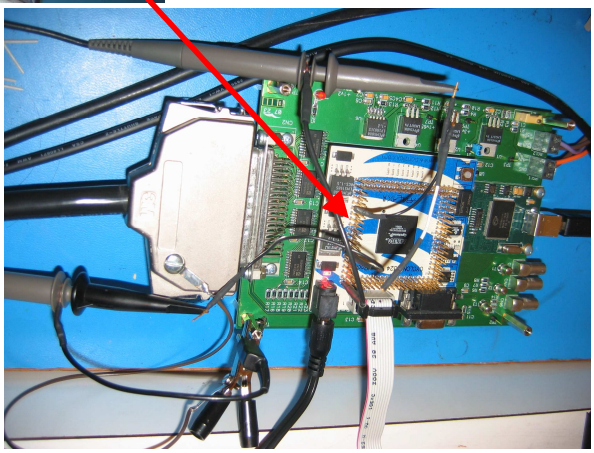


The LPNHE test bench used to test the functionality of the new chip. The chip is located on a special test board; a sequence of test parameters is sent as input to the chip in order to test it.

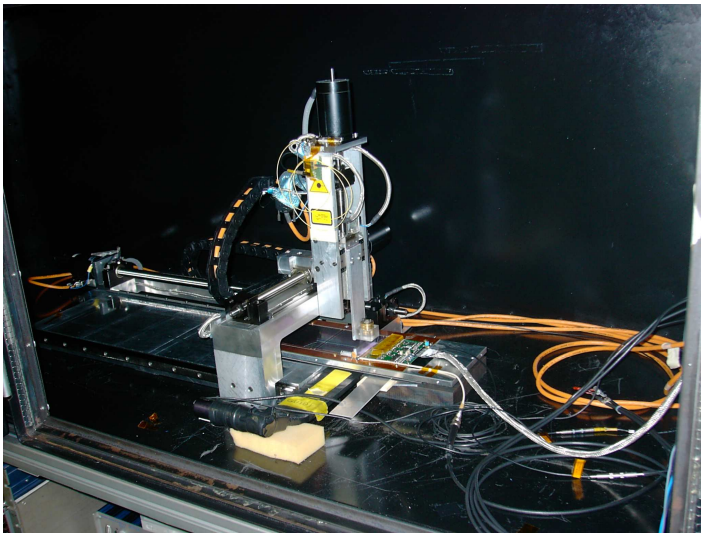


The new digitized FE readout system and the associated new DAQ system were developed and tested at the Lab test bench as shown here in front.
The bottom left photograph shows the FE board equipped with 4 chips, i.e. 16 readout channels.
The bottom right photograph shows the DAQ board equipped with an FPGA and an USB interface.

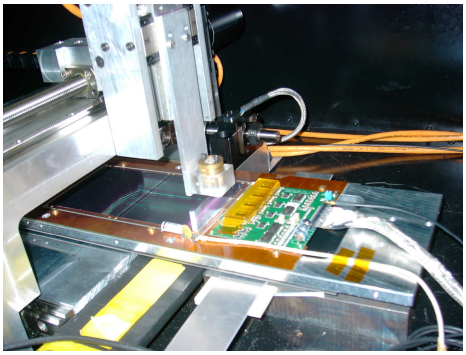




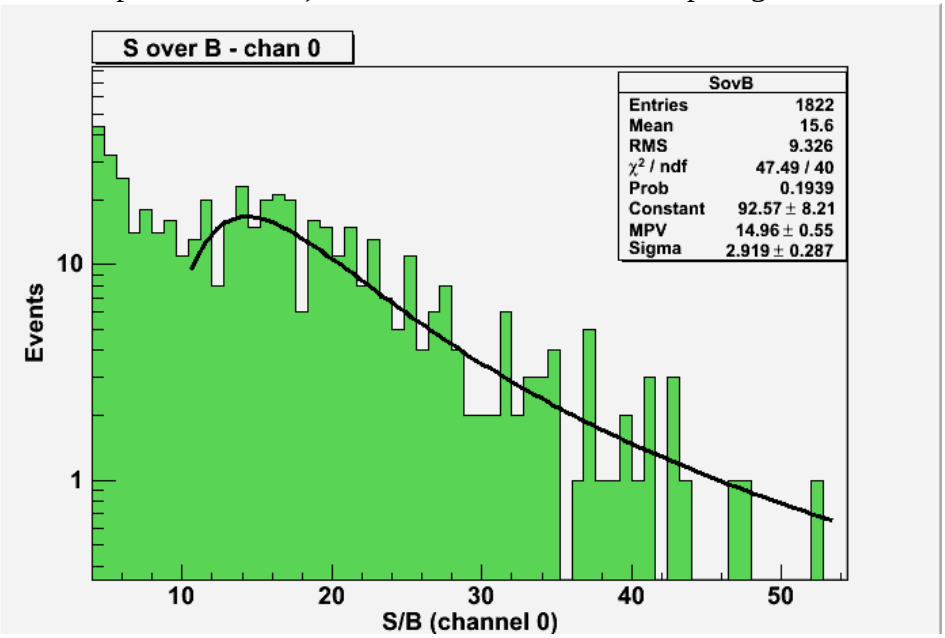
A test bench including a motorized 3D table, a DAQ system LabView based, is used to test the new modules and the associated new FE readout chips. The Faraday cage in which the overall set up is installed in shown in the pictures here below.



Test set-up for the electronics and the new modules at the LPNHE Lab test bench.



The photograph (left),here above, shows the 3D motorized table in the Faraday cage used to test the silicon modules (even long ladders up to 1m long) excited by a Laser diode or by a Sr9 radioactive source. The photograph (right) zooms on the HPK module read out by the new SiTR_130-v1 chip.
The measured S/B is shown in the Figure here below for one channel of the SiTR_130-v1 chip reading out the HPK module excited by a Sr90 radioactive source. The S/B measured value (MPV = most probable value) is of 15 in this case for a strip length of 18cm.

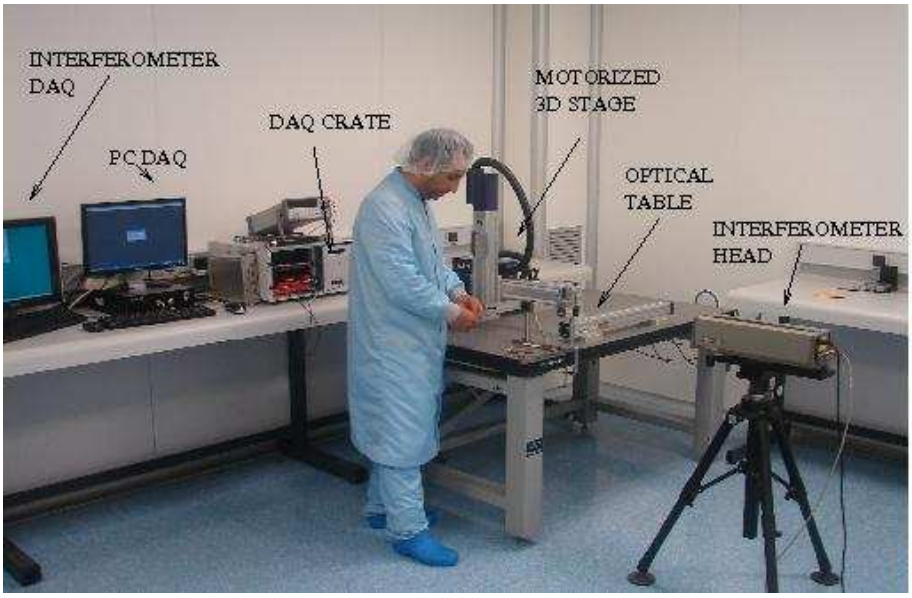


Other test results with the previous SiTR_180 prototype were reported at the LCWS07 workshop [23].
[23] W. Da Silva and F. Kapusta, on behalf of the SiLC Collaboration, *Source Test of the 180nm chip with GLAST and CMS sensors*, in Proceedings of the LCWS07, DESY-Hamburg, June 2007.

III-2-2: Alignment test bench

IFCA counts with a metrology laboratory where test of components of the link alignment system of CMS has been carried out [24]. The lab surface is 145 m^2, and has a free diagonal path of 27 m plus reinforced concrete floor independent of the structure of the building. The equipment includes 3 and 6 m long granite benches, antivibration tables with charge compensation systems, and a high precision 3D coordinate measuring machine.

Attached to it, there is a clean room (class 10000) that allows working under controlled temperature and humidity conditions, with a conducting floor. Inside this room, the optical testing of the HPK and CNM alignment sensors will be executed. The testing will be completed with laser scanning, cosmic and beta-source test in a dedicated test bench, currently being commissioned (see picture here below).

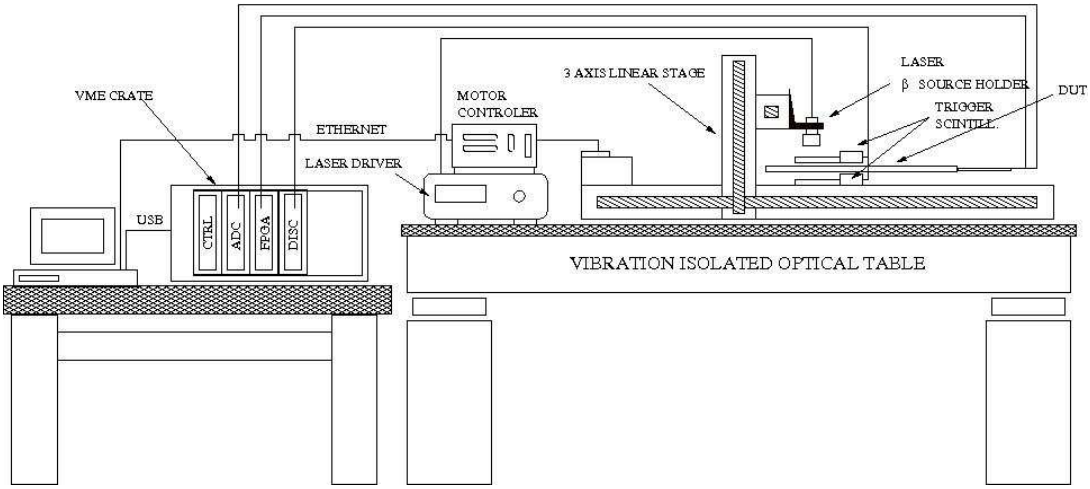


Components used for optical characterization and scanning of transparent Si microstrip- detectors

Motorized 3D stages.

The assembly consists of 3 axes motorized linear stages for characterization of large modules; the moving head can scan a volume of 500mm x 300mm x 200mm with a nominal precision of 10 μm. The linear stages [25] are controlled from the PC via an ethernet interface, see Figure here below

By standard interferometric techniques, used for the calibration of machine tools [26], we expect to achieve a sub-micrometric accuracy on the measurement of the moving head. This calibration will allow us to measure with sub-micrometric deviations from the ideal stage displacement.

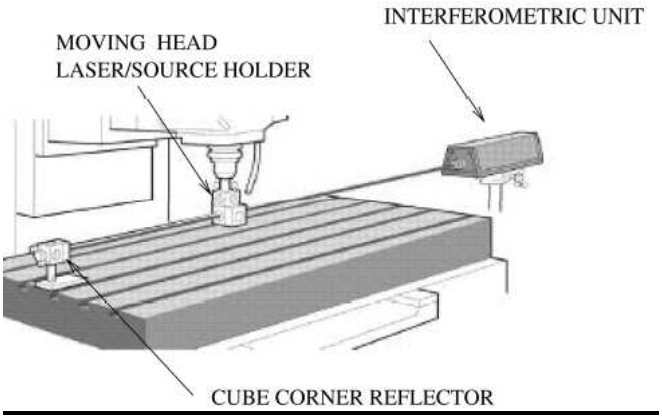


Detailed sketch of the setup and connections between the components.

DAQ system.

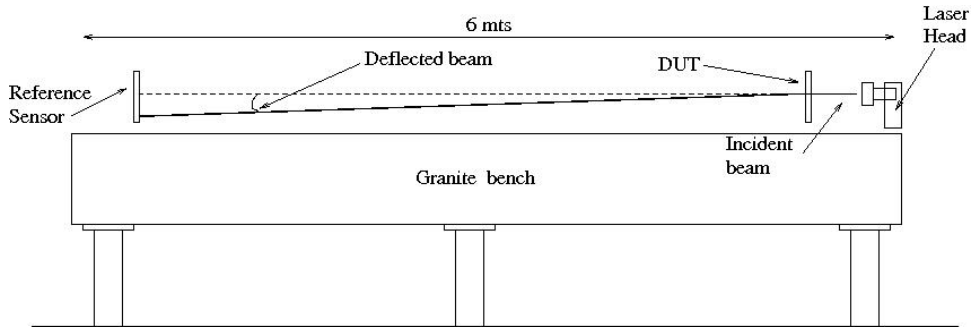
We are currently using a VME based DAQ system for the readout of sensor prototypes. The VME master is a CAEN-V1718 module that can be operated from the USB port of the standard PC. The DUT is readout by the ADC module CAEN-V895B, a 14 bits, 100 MS/s digitizer; the readout sequence is driven by the CAEN-V1495 board a multipurpose programmable board interfacing a FPGA chip to the VME bus; the DAQ system is completed with a leading edge discriminator board CAEN-V895 implementing the trigger logic.

Laser system.



Laser characterization of the sensor prototypes will be carried out both in the previous described test bench and on the granite bench. In the former test bench, the overall sensor response and single strip characterization will be carried out. The granite bench will be used for measurement of the deflection angle of the transmitted laser beam going through the DUT. The precise determination of the deflection angle requires a long distance between the DUT and the "reference sensor", see Figure here below

For single strip laser testing, a 1060~nm DFB diode laser [27] coupled to a fiber and using a [28] collimator that will allow to create beam spots with a diameter of few microns.



Alignment bench configuration for measurement of beam deflection introduced by the DUT. The DUT is mounted in a 2D or 3D linear stage

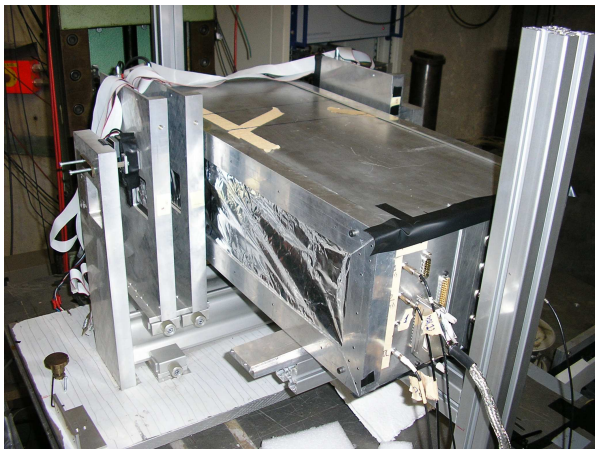
[24] M. G. Fernandez et al., "*Semitransparent amorphous silicon sensors for the CMS alignment: an in-depth study*", NIM A440, Issue 2, 1 February 2000, Pages 372-387
[25] Adept Technology, Inc. http://www.adept.com/products/details.asp?pid=65
[26] Agilent 5529B Laser Calibration System.
http://www.cdmeasurements.co.uk/agilentlasers_basic_system.htm
[27] Fermion I series, Micro Laser Systems, Inc.
http://www.microlaser.com/Fermion1_Specs.html
[28] Schafter + Kirchhoff, GmbH. http://www.sukhamburg.de/download/fk60fc_e.pdf

II-3: Test beams

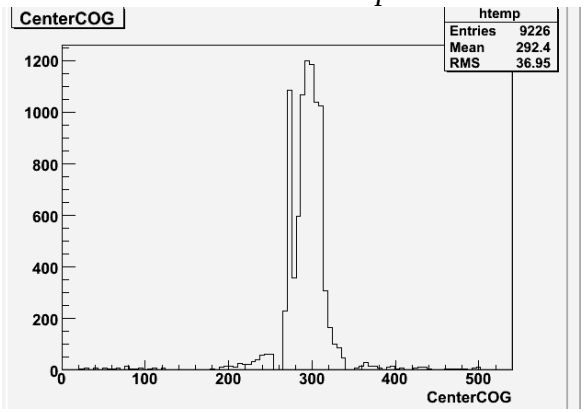
An active program of test beams was launched at the end of 2006 and implied a lot of work during the overall last year. It will proceed on these next years essentially following the E.U.

EUDET framework and programme of work. Despite being a European project, it should be pointed out that the facilities and all the infrastructures are also available for all the SiLC partners included the non European ones.

II-3-1: Test beam in DESY in 2007



Silicon modules in the Faraday cage inserted in between the beam telescope at DESY



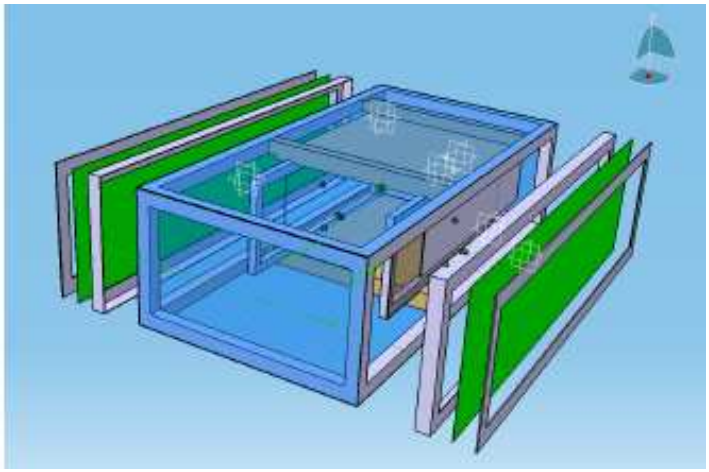
Online beam profile from Silicon layer read out by VA1 chips

Two weeks of tests at DESY in June 2006 were achieved in continuation of those made on November 2006 [3].
The attempt was made to measure the S/N ratio for the first SiTR_180 chip that included only the analogue part up to the comparators and to compare with the VA1 reference chips.
In parallel at the LPNHE Lab test bench was tested a new module made of 3 CMS sensors and with 16 channels read out with the SiTR_130-v1 chip (see II-2-1).
Associated to the new chip with digitized readout, a new DAQ hardware based on an FPGA board plus USB interface was tested. The new DAQ software was tested as well. But it was not possible to have this overall new system ready in time for the DESY test beam in June.
However it was a good training camp for the October test at CERN.

II-3-2: Test beam at CERN in 2007

The test beam at CERN, was achieved at the H6 SPS beam from October 10 to 22, 2007. The main goals were to test prototypes of the new HAMAMATSU (HPK) large size sensors that were just delivered on October 1st and the new front readout chips made by LPNHE and LAPP, using CMOS 130nm UMC technology. Related to it a completely new DAQ systems both hardware and software was developed. Moreover it was a combined test with the EUDET pixel telescope. Indeed SiLC and the EUDET telescope performed the first EUDET combined test beam (see ILCNews article of January 2008).

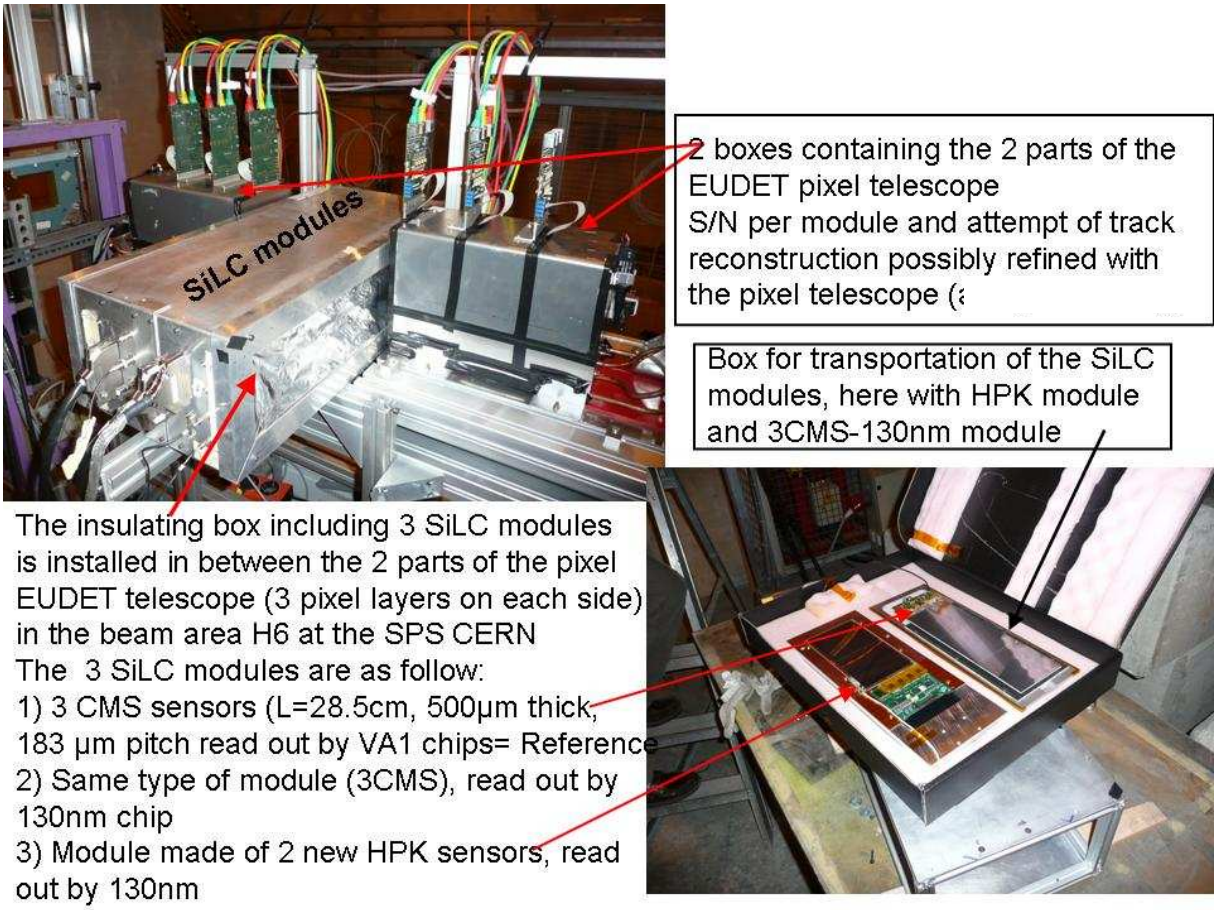
Three Silicon modules with their related FE readout electronics and DAQ constituted the tracking system that was tested this year.



The three Silicon modules sitting inside the Faraday cage were precisely positioned thanks to rails in which they were located as shown in the picture here on the left.

. The detailed drawing of the Faraday cage where the three Silicon modules were installed

Details of the overall system installed and tested in the H6 beam are given here below. A photograph on the left here below, shows the set-up and the Silicon tracking system installed in between the two parts of the EUDET telescope.

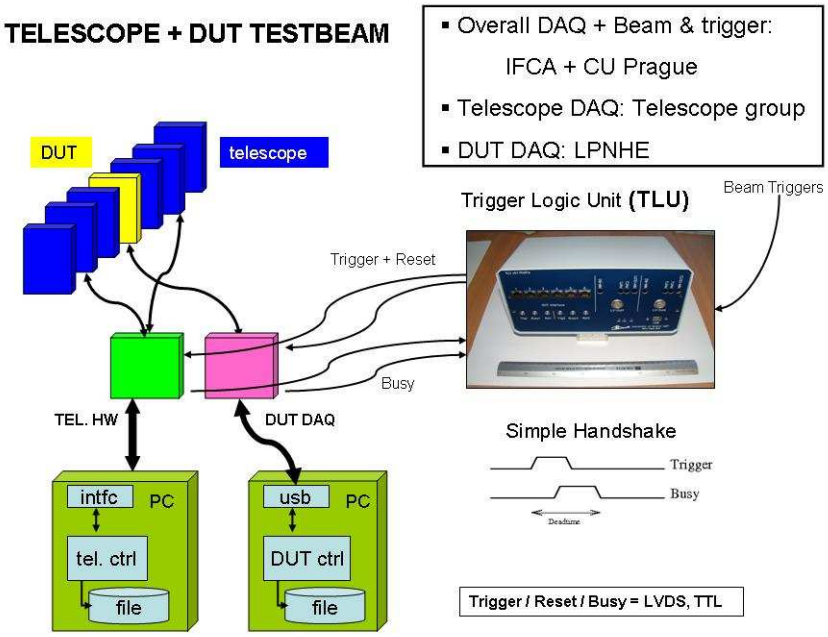


Photographs of the test set up at the H6-SPS beam (top left) and of the modules in their transport box (bottom right)

The new HPK microstrip sensors are single-sided, 9.15 x 9.15 cm^2, thickness 320µm, and 50µm pitch. One out of the 3 modules installed in the SiLC Faraday cage was made with these new sensors that were delivered just few days before the start of the run (see also photograph bottom left here above). The collaboration with the Bonding Lab at CERN and

especially of A. Honma, I. McGill and M. Moll was essential in preparing both the Silicon modules and their FE boards.
The chip SiTR_130-v1, made in CMOS 130nm technology was used to equip the FE borads for the HPK module and one of the 3-CMS modules (see I-3-2 and II-2-1). It included the complete FE and readout chain which processes the detector signal including A/D conversion. Each chip prototype was reading out 4 channels. Four such chips were installed per F.E. board.

A new DAQ system was developed able to read the two different Silicon modules readout systems, namely one read out using the VA1 analogue chips (from IDEAS used as reference) and the other one being developed to read out the digitized information provided by the new 130nm chip prototypes. This DUT DAQ system was associated to the EUDET pixel telescope DAQ and to the timing/trigger unit TLU. This is a new (EUDET) timing unit used to synchronize both detector systems (Telescope and DUT) with the beam trigger. A schematic view of the overall DAQ system is shown in the Figure here below.



Schema of the DAQ system developed for the SPS test beam in October including the EUDET telescope DAQ system and the SiLC DAQ system for the Silicon detectors (DUT)

The installation took one day and we spent about three days in order to have everything running smoothly and well checked. Some SiLC collaborators participated to the test beam of the EUDET telescope in order to be trained to run this new device as well as the TLU.
The used beam was 120 GeV π beam and some runs were done with reduced multiplicity by closing the beam slits. Also some runs were taken varying the running conditions on the FE electronics (changing the low voltage setting around the nominal value for the FE chip) and the bias voltage on the sensors.
Some very basic and preliminary plots were made available by the analysis/monitoring team, during the data taking. They are shown here below; the four uppermost plots are from the module which has all the 512 channels read out with four VA1 chips. It serves as reference but also it shows the beam signal and thus that everything in the DAQ system is properly working. This series of plots are shown in the figure here below.

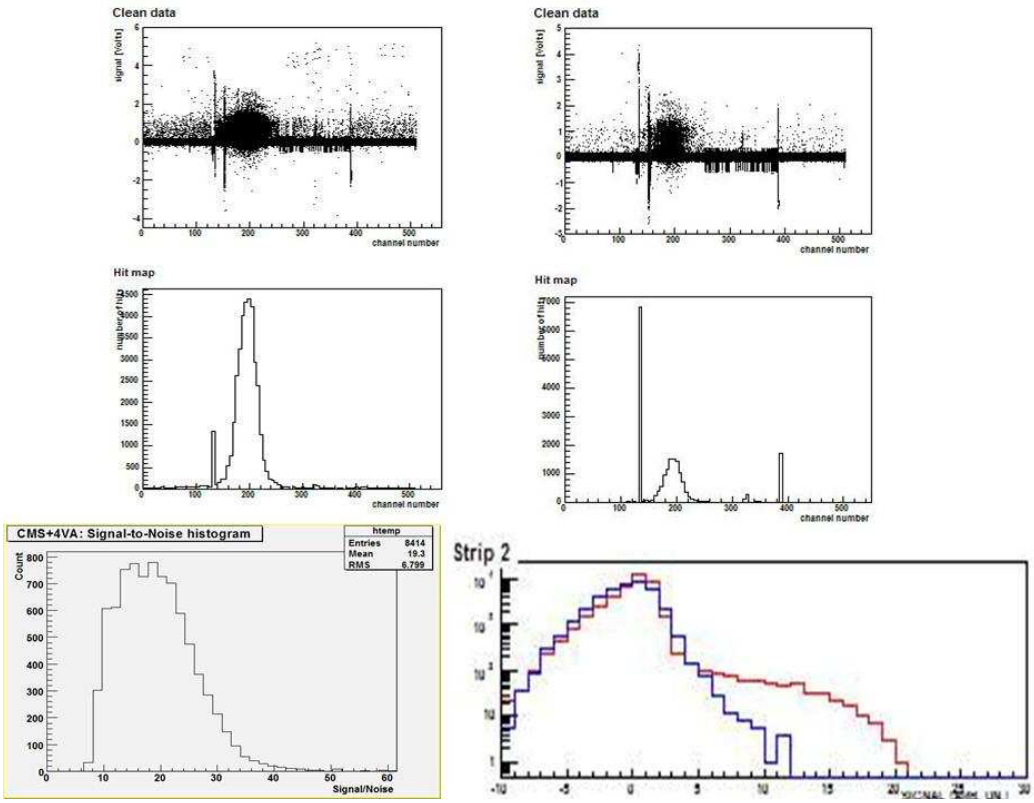
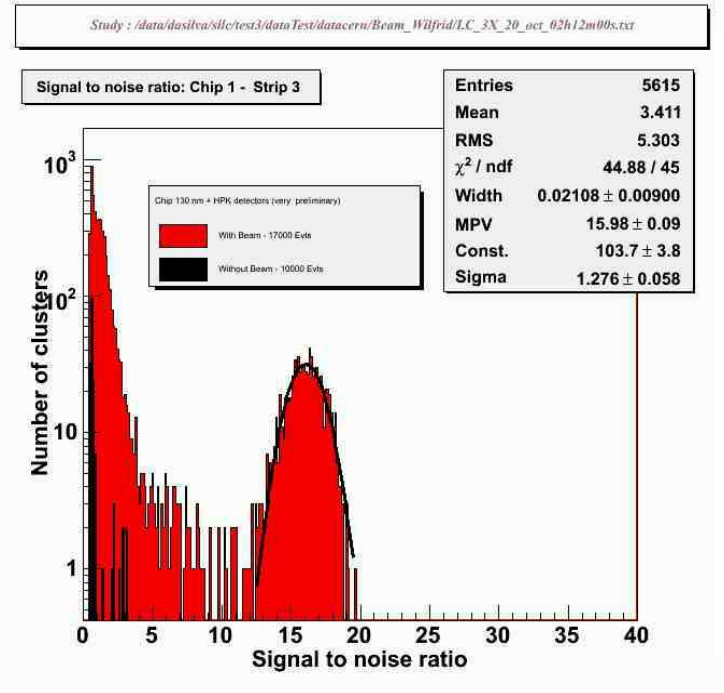


Fig.5. Preliminary plots: the top two plots show the raw data distribution for the reference module read out with VA1chips (512 channels) and the CMS large TOB sensors that equipped this module (left is with high multiplicity beam, right with low multiplicity). The next two plots show the hit maps for the two cases mentioned here above; the last bottom left plot shows the Signal to Noise ratio for the reference module peaking around 20 and the right plot shows the pedestal (blue) and the signal (red) as given by one channel of the new FE chip (130nm).

A detailed analysis of the data was performed afterwards. The most important result is the determination of the S/N ratio for the new chips and the new HPK sensors [29, 30].



A typical S/N value (MPV= maximum probable value) of 16 is obtained for one single channel. This is shown on the plot here on the front left. It varies typically from 13 to 18 per channel.

When gathering at least 2 channels it increases to more than 20. This is a quite good result for strips 18.3cm long and also compared to the results obtained with the VA1 chips and based on all the channels and not a single or very few channels.

More results are extracted from the large amount of test beam data. Besides, a series of additional tests with the Sr90 radioactive source have been lately taken at the LPNHE test bench and are under analysis. A report will be soon produced with a complete series of results combining both those from the CERN test beam and those from the Lab test bench. Together with the detailed characterization of each block of the SiTR_130-v1 described in I-3-2, these latest results will give a complete view of the full characterization of this new device and of its performances.

To conclude this test beam at CERN was quite successful and demonstrate that the SiLC test beam crew has acquired now a good experience on the design, preparation, setting up and analysis of data for these test beams. Moreover it was the first experience of a combined test beam (Vertex EUDET prototype plus our Silicon DUT) in the ILC community.

The list of people that participated to the test beam is given at the end of this document.
The sharing of tasks for the preparation and the running of this run is indicated in the Table 1.

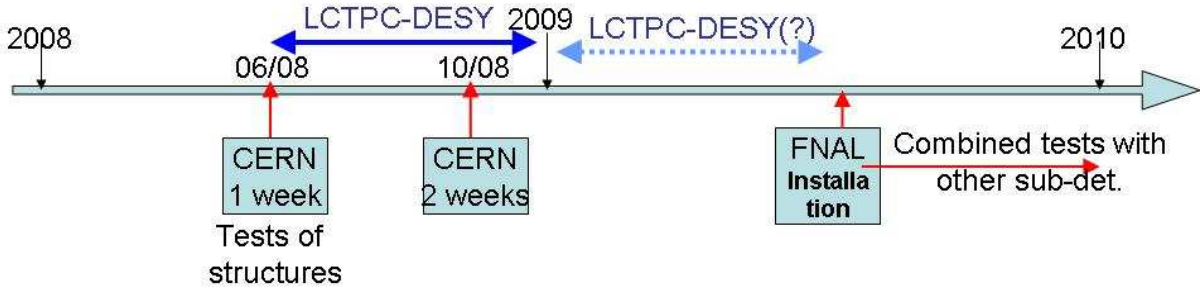
Topic	Team(s) in charge	Other collaborating teams
Sensors	HEPHY	IEKP, LPNHE
Module construction	IEKP, LPNHE and CERN	
FE Electronics	LPNHE	
DAQ Hardware: - Front-End boards - FPGA boards - TLU unit - cabling	 LPNHE LPNHE EUDET LPNHE	 CERN bonding Lab Barcelona University CuPrague, IFCA, Geneva U.
DAQ software - General software - Telescope software - Silicon tracking system	 IFCA Geneva U (EUDET telescope) LPNHE	 Barcelona University
Installation	IFCA, CuPrague, LPNHE	EUDET Telescope
Data taking	IEKP-Karlsruhe, HEPHY Vienna, LPNHE Paris, Cu Prague IFCA Santander, Torino-INFN and Uni of Torino+ Geneva*	
Analysis	Cu Prague	LPNHE Paris

Table 1: Sharing of tasks for the preparation and the running of the SiLC beam test in 2007.

[29] W. Dasilva and F. Kapusta, on behalf of the SiLC collaboration, *Preliminary Results of the 130nm chip CERN test beam*, presented at the Sixth SiLC meeting in Torino (Italy), Dec 2007, in: http://www.silc.to.infn.it/doc/papers/wilfrid_dasilva.pdf
[30] A. Savoy-Navarro, on behalf of the SiLC Collaboration, *The latest developments of the SiLC Collaboration*, presented at the TILC08 Workshop in Sendai (Japan), March 2-7, 2008, in http://ilcagenda.linearcollider.org/conferenceOtherViews.py?view=standard&confId=2432

II-3-3: Test beams schedule in 2008-2009

Over these two years, the SiLC test beams will occur at three test beam facilities. A preliminary schedule of these test beams as they are presently foreseen is given in the figure here below. In 2008 the test beams will be done both at CERN and at DESY. In 2009, the test beams will be done essentially at FNAL and whether or not there will be a continuation of the tests with the LCTPC at DESY is still to be defined.



II-3-3-1: Test beam at DESY in 2008

There will be a combined test beam in collaboration with the LCTPC collaboration. It will start with cosmics in summer 2008 and will proceed with a test beam starting in September when the DESY test beam facility is again available. This test beam was already described described in I-1-2-1 and references there in. The preparation on the SiLC side is on-schedule.

II-3-3-2: Test beam at CERN in 2008

Two requests to the CERN-SPSC for test beam have been submitted by the SiLC collaboration on November 15, 2007 for test beam allocation in 2008 and have been actually accepted.

The system to be tested in 2008 at CERN will include a set of new Silicon modules that will be tested with a beam telescope; the EUDET telescope will be used, in a therefore combined test beam, for the test beam in June and before its removal back to DESY. Many improvements are expected with respect to this year test beam. They include:

1) New sensors with eventually some ones based on novel 3D technology (3D planar microstrip prototypes) Comparison of performances in terms of S/N and also spatial resolution will be performed between the different modules.
2) New SiTR_130-96 FE chips that will include the full readout chain i.e. a test pulse included now in the FE chip itself, power cycling and some upgrades with respect to the present version, namely: in the shaper, the sparsifier for zero suppression, the analogue pipeline. Moreover the new chip will include the digital part (managerial part) not part of this present version. Performances of this new chip will be compared with the reference ones (VA1 chip) and with the ones of the chip tested this year, in terms especially of S/N response.
3) A new DAQ system based on a new FPGA board to pilot the data taking of the overall DUT system (this year we had one FPGA board per module).A new DAQ software able to efficiently handle the functioning of the telescope and the DUT is also being developed.
4) A new monitoring system to monitor the functioning of the system will be prepared as a direct outcome of the analysis of the present data.
5) A new alignment system based on especially treated sensors (provided by HPK) and an IR laser system.
6) A new insulating box made of new material with the requested thermal and electrical insulating properties.
7) A track reconstruction programme able to combine the track found by the DUT with the ones found by the telescope.

A first beam period of one week is allocated by the SPSC from May 31 to June 4, 2008. This first beam period will be concentrating on testing the new HPK sensors with test structures that we ordered in 2007. These structures contain strips with different widths and different number of intermediate strips. By using the very precise EUDET telescope as reference, one could measure the resolution of the different strip geometries included in the structure very precisely, even under different DUT angles. Since these parameters are very dependent to multiple scattering, the high energy beam of the SPS is a very good opportunity for testing resolutions in order of few microns. The result would allow determining the sensor characteristics providing the best resolution.

The details of the sensor structures that were delivered by HPK in October 2007, and that will be tested in this first beam test period are discussed in I-2-1; The readout system used for this test will be based on APV25 system test available among the SiLC collaborators also members of CMS, thus independently of the new FE chip date delivery. This new chip will be tested in the second period allocated in October 2008.

The list of topics 1) to 7) are under development and should all hopefully be ready by October 2008. This is the period of time where we would like to have our second beam test at CERN SPS with duration of two weeks. Back up solutions are studied or already foreseen in case one of these topics fails to be ready in time.

The teams that already register to participate to the test beam preparation and data taking are: Barcelona University, CNM-IMB/CSIC, IEKP Karlsruhe, Obninsk State University, LPNHE Paris, Cu Prague, IFCA Santander, Torino-INFN and University; HEPHY Vienna, some other teams already indicate their interest in participating to this test beam.

The present sharing of tasks is listed in the Table 2 here below

Topic	People in charge	Other team collaborating to it
Sensors Novel technology	HEPHY VTT and HIP	IEKP, LPNHE, more to come HEPHY, LPNHE
Module construction	IEKP and LPNHE	More to come
FE Electronics New chips: VA1 reference APV25 reference	 LPNHE LPNHE IEKP Karlsurhe+HEPHY	 Barcelona U. and LAPP
DAQ Hardware	LPNHE, IEKP, HEPHY(for APV25)	Barcelona U.
DAQ software	IFCA	LPNHE and CU Prague
Monitoring system	tba	CuPrague, IFCA, LPNHE
Alignment	IFCA	IMB-CNM/CSIC
Insulating box	Obninsk State University	
3D Table	Torino-INFN & Torino Uni.	
Analysis software	Cu Prague	LPNHE and more to come
Track reconstruction	tba	Several teams
EUDET telescope running	IFCA	Cu Prague,EUDET telescope

Table 2: Sharing of tasks for the preparation and running of the SiLC test beam in 2008.

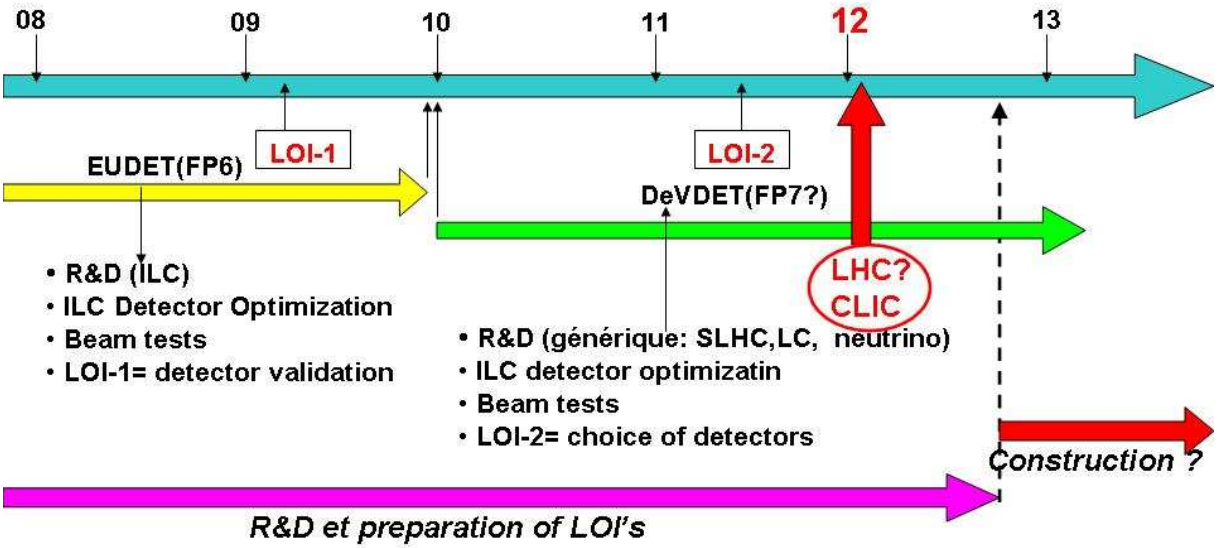
II-3-3-3: Test beam at FNAL in 2009

The SiLC collaboration will join next year the combined test beam that is launched this year by the CALICE collaboration at FNAL test beam area and that will continue over the next year. The so-called 4-layer prototype described before will be installed in this test beam. The installation is foreseen around June 2009 and the installed Silicon device will be available for the overall combined effort until the end of 2009. This is also in the framework of the E.U. EUDET project. It is foreseen to have our US and Asia colleagues from SiLC and also other colleagues from SiD to join this effort. This is under discussion. The preparation/construction phase for this test beam will start in the second half of 2008.

Here below is the list of people that contributed to the beam test at CERN in 2007:
University of Barcelona: *(David Gascon, Jordi Riera and Xavier Vilasis)*
IEKP Karlsruhe: (*Peter Blum, Frank Hartmann*), Martin Frey and Karl Heinz Hoffmann,
IFCA Santander: Javier Gonzalez Sanchez, Marcos Fernandez Garcia, Ivan Vila,
Cu Prague: Zdenek Dolezal, Zbyniek Drasal, Peter Kvasnicka ,
HEPHY Vienna: (*Stephan Haensel)*
Torino University: Diego Gamba and Mario Pelliccioni,
LPNHE Paris: Catalin Ciobanu, Wilfrid Dasilva, Jacques David, Marc Dhellot, Jean Francois Genat, Jean Francois Huppert, Frederic Kapusta, Thanh Hung Pham, Aurore Savoy-Navarro *(Guillaume Daubard, Patrick Ghislain, Francois Rossel, Rachid Sefri*),
(In parenthesis are people that contributed in the preparation but didn't participate to the test beam at CERN itself, i.e the installation and data taking).
CERN Bonding Lab: Alan Honma, Ian Mc Gill and Michael Moll
EUDET telescope Ingrid Gregor, Tobias Haas and collaborators and special thanks to Emlin Corrin and Daniel Haas.

PART III: Participation to the LOI's, organization and perspectives

SiLC as all the other main ILC R&D collaboration has to fit with the evolution of the ILC roadmap which we summarize in the figure here below.



SiLC and ILC Roadmap (present status)

III-1: Milestones and Participations to LOI's

The main challenge in the present ILC schedule for the period going from 2008 to 2012, is the **two-stage LOI procedure**. It is mandatory for SiLC to actively participate to each stage of the LOI procedure, with stage 1 (LOI-1) being the validation of the detectors and stage 2 (LOI-2) being the choice of the detectors that will finally go for construction.
Presently three detectors are intending to present an LOI: the ILD, the SiD and the 4th concept detectors. ***All three have expressed their interest in the SiLC collaboration work***. Indeed each of these detectors have a tracking system that includes Silicon components (ILD with the Silicon components completing the central TPC tracker as described in this present status report), the SiD which is a all-Silicon tracking system and the 4th concept which is looking for what they call the "*best tracking system*".
Another important point in this schedule is the **E.U. EUDET program** that gives support for part of our R&D activities, valuable framework especially in terms of test beam facilities, and which fits well with the first part of the ILC roadmap, namely until end 2009. For the period 2010-2012, another project is launched and should hopefully provide, if accepted, additional support for this second period as well as an enlarged collaborative framework in the European space for research with outcomes for our non European partners too.
Finally and since the very beginning SiLC has emphasized the strong synergy between the ILC and the LHC and its upgrades. This is especially true in this domain of R&D. The collaboration SiLC has already developed strong connections with LHC. It will be certainly reinforced in these years.

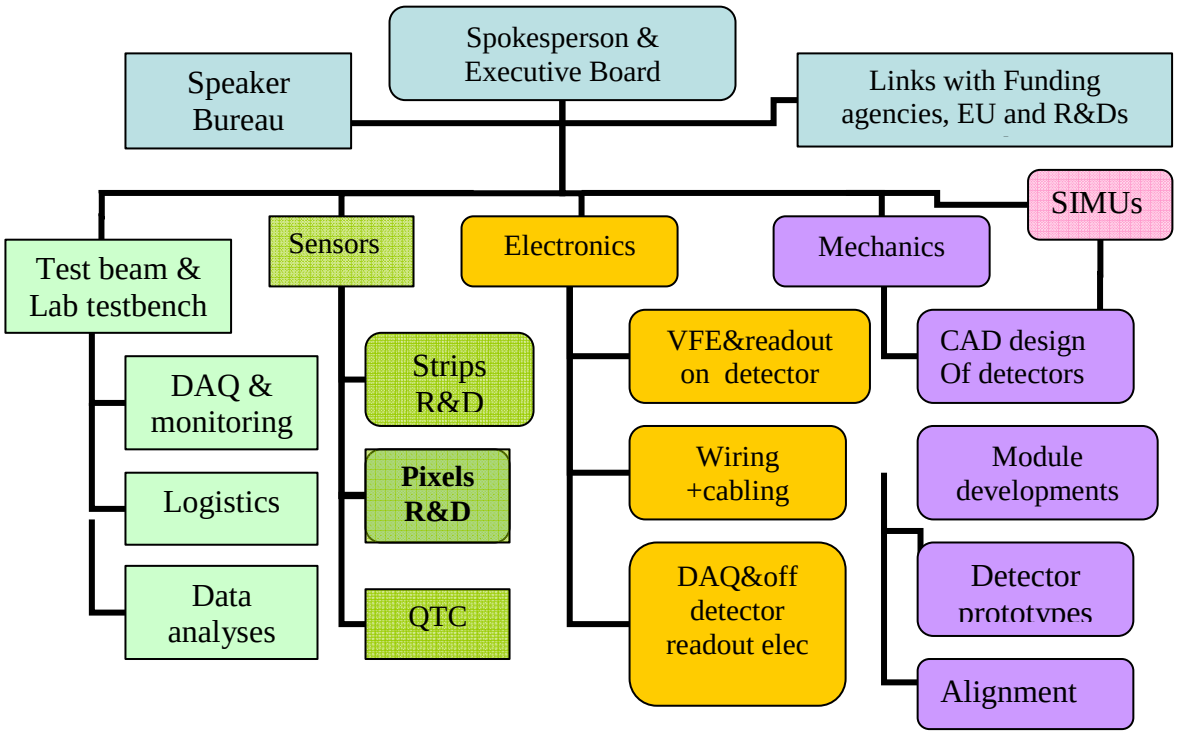
The SiLC R&D has a well-defined work plan [3 and addendum] for developing all the needed R&D aspects in these coming years, especially until 2010. It will be carefully readjusted year to year and even 6 months per 6 months in order to cope with various important issues still unknown. This flexibility is mandatory because the R&D tackles high tech issues and because of the still possible changes in the ILC overall schedule in these next years and up to 2012.

In order to give the needed contribution to the detector LOIs, the SiLC collaboration is working on all the R&D aspects described in part I. Moreover the development of the tools is essential as well. Simulations studies are instrumental for the optimization studies that are starting for the three detectors; SiLC has taken responsibility in the Silicon tracking for the ILD and prepared the needed framework.
A certain number of SiLC teams are interested in the other concepts and will devote time to study the all-silicon tracking alternative or other possible scenarios with gaseous detectors plus Silicon tracking.
It was clearly stated at the TILC08 [30] and taken also as conclusion in the summary talk on "Vertexing/Tracking" by Takeshi Matsuda [31], that "*SiLC is a transversal R&D activity. It intends to play a major role to study and compare the tracking alternatives proposed for the ILC with a joint optimization task force*".

III-2: Organization of the collaboration and sharing of tasks

The organization of the overall R&D collaboration in terms of definition of tasks, of responsibility or sharing of resources and of defining milestones is being reinforced this last year. This is driven by the increase in interests of the teams to actively participate to the R&D effort and by the increase in amplitude and challenges of our R&D activities. Moreover the advances made in various R&D aspects and the developments of collaborative efforts with industrial partners impose to reinforce as well our collaboration bylaws. This is presently in

progress via MoU's and NdA's, MTA's procedures that are being established/defined. The general present distribution of tasks is given by the flow diagram here below and the Table 3 that specifies the names of Institutes currently sharing these tasks.



Main topic	Specific items	Coordinator	Participating Institutes
Sensors	Microstrips	HEPHY	VTT-HIP, LPNHE, IFCA, Liverpool U., HPK-Photonics
	Pixels-DEPFET	IFIC	CU-Prague,
	Other	tba	tba
Electronics	FE readout	LPNHE	BU Barcelona, LAPP, SCIPP-UCSC
	DAQ (DUT)	LPNHE	HEPHY (APV25), LPNHE,
	DAQ (general)	IFCA	Barcelona U, CU Prague
Mechanics	Modules	IEKP	IFIC, Korean group, Liverpool Uni., LPNHE
	Prototypes	tba	IEKP, LPNHE, Liverpool U., IFIC, Torino U.,
	Alignment	IFCA	Michigan U.
	Cooling	OSU	LPNHE, Torino U., IFIC
Simulation		IFIC(M Vos) OSU(Saveliev)	CU Prague, HEPHY, IFCA, KOREAn Group, LPNHE, UCSC
Test beams	DESY	Z. Dolezal	See Table 1 and 2
	CERN	A.Savoy-Nav. M. Fernandez	See Table 1 and 2
	FNAL	tbd	Table 1 and 2 + non E.U partners
	DAQ software	IFCA+LPNHE	tbd + other colabrators (EUDET et al.)
	Analysis/monitoring tasks	tbd	CUPrague, LPNHE, IFCA

Table 3: current sharing of tasks and responsibilities

Collaboration Meetings:
The organizers of the ECFA Workshop in Vienna in November 2006, initiated the SiLC collaboration Meetings. Since then two collaboration meetings are held in the different Institutes that are collaborating to SiLC. They last 2,5 or even 3 full days. After Vienna, Paris, Liverpool, Barcelona, two SiLC Collaboration meetings have been organized in 2007. The Fifth SiLC Meeting was organized by the Charles University in Prague on April 25-27 (see http://www-ucjf.troja.mff.cuni.cz/ilc/silc/meeting/html/progr.html) and the Sixth SiLC Meeting in December at the University degli Studi in Torino (see http://www.silc.to.infn.it/ and an article on the ILCNews in January 2008), with an attendance of 25 people in Prague and about 50 in Torino.

Our collaboration meetings are an occasion to also review what other experiments are/have been doing (especially the LHC experiments: ATLAS, CMS, LHCb and ALICE). People from other sub detectors are also invited as the LCTPC group in Barcelona.
In Torino meeting people from the SuperB factories were invited as well as several teams working on various aspects of the pixels new developments, especially on the 3D, and representatives of the 3 detector concepts as well.
In 2008, the two scheduled collaboration meetings will be held at the very end of May in Moscow (organized by V. Saveliev) and mid December (organized by A. Ruiz-Jimeno) in Santander.

[31] T. Matsuda, *A brief Summary of the Talks in the Vertex/Tracker Parallel Sessions*, at the TILC08 Workshop, Sendai (Japon), March 2-7, 2008 and in:
http://ilcagenda.linearcollider.org/getFile.py/access?contribId=21&sessionId=2&resId=1&materialId=slides&confId=2432

Concluding remarks

Over this last year, the SiLC R&D collaboration has achieved in many ways an impressive step forward. Advances in various fronts such as:

- The sensors: new microstrips with collaborative effort of founders including HPK; novel 3D-planar technology, developed expertise/interest in new pixels.
- The FE readout chips in 130nm CMOS technology fully characterized and proven to work in realistic test beam conditions.
- Design, layout and sending to foundry of the next version that will equip large protos.
- Wiring of the chip onto the detector is in progress with Industry.
- Gained expertise on all aspects of test beams (DAQ, analysis of data, first combined test with EUDET beam telescope).
- Detector prototypes are built and tested at Lab bench and test beam (DESY, CERN);
- Alignment and Cooling
- A task force on simulation, gathering expertise from various Labs in a coherent way and impact on the optimization of detectors for LOIs (ILD) and more to come.
- Developing collaborative effort on simulation with the other sub-detectors and all detector concepts.
- Building up the collaborative framework with two collaboration meetings per year in different places; real forums, exchange of knowledge and expertise, definition of tasks and responsibilities.
- Enlarged collaborative effort from already participating teams but bringing now more people and expertise to this R&D collaboration, because increased interest in the R&D and decrease involvement in the LHC construction.

Apart from a valuable expertise they reinforce the synergy between ILC and LHC. This is to the benefit of both the LHC upgrades and the ILC R&D as it is already appearing quite clearly. It gives SiLC an additional asset.

But in order to allow us (as all the other ILC R&D activities) pursuing successfully our R&D program, it is essential that we continue getting the needed means in terms of funds and persons in the forthcoming years and despite the increased competiton with other projects in the field..