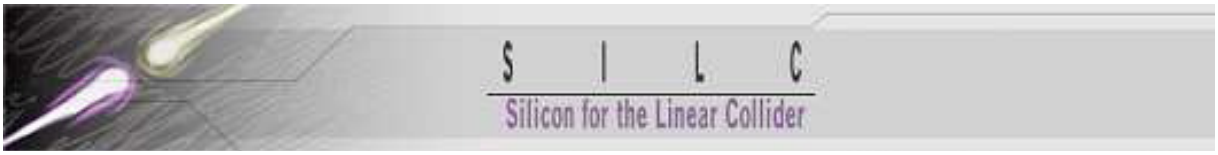

Status Report to the PRC DESY, October 14 and 15, 2010

Submitted, on October 8, 2010

SiLC (**Si**licon Tracking for the **L**inear **C**ollider)

University of Michigan, University of Barcelona, IMB-CNM/CSIC, HIP University of Helsinki, VTT-Helsinki, IEKP University of Karlsruhe, Moscow State University and SiLab, Obninsk State University, LPNHE University Pierre and Marie Curie/CNRS-IN2P3, Charles University in Prague, SCIPP and University of California in Santa Cruz, IFCA-University of Cantabria/CSIC, Yonsei University, Korea University, Seoul National University, SungKyunKwan University, Kyungpook National University, INFN-Torino and University of Torino, Rutherford Laboratory, KEK in Tsukuba, University of Tokyo in Tokyo, IRST in Trento, IFIC CSIC–University of Valencia, HEPHY-Academy of Sciences in Vienna.

Abstract

This status report reviews the main achievements of the SiLC Collaboration these last two years. The previous results were reported in details in the proposal to the ILCSC R&D Tracking Panel (February 2007) and in the previous status report to the PRC on April 2008. Advances on sensors R&D are achieved in several ways. The new microstrip sensors developed by collaborative contacts with HPK Photonics are the current baseline and other firms are interested as well. VTT in Finland and IRST in Trento are producing novel active-edge strip sensors. CNM-IMB and IFCA are developing novel alignment friendly sensors with high transmittance. SiLC teams are starting to explore new pixel technologies. After the FE readout chip prototype developed in 130nm CMOS UMC technology by LPNHE and successfully tested at the test beam at CERN, a complete mix-mode 128-channel version is under design with important preliminary results. These are the chips that will equip Silicon tracking prototypes in the coming years. HEPHY in collaboration with ITE is developing strips sensors with integrated pitch. SiLC was instrumental in the write-up and technical support of the Letters of Intent of the detector concepts and especially of the ILD LOI. The integration issues were studied in great details including already realistic solutions. Major advances in test beam activities are achieved at the CERN-SPS with various Silicon prototypes and complete Silicon test infrastructures and at DESY in the combined test beam with the LC-TPC prototype. A major effort is underway on the detailed simulation of the Silicon tracking with the installation of all the components of the Silicon tracking system in the MOKKA/Marlin framework. The goal is to include a realistic design of the Silicon tracking system for the simulation studies for the DBD report in 2012. The simulation studies of the very forward part are well advanced. The development of the Si tracking reconstruction is undergoing. These last two years also, activities related to the preparation of the CLIC CDR were launched as well as contributions to starting (BELLE II) or near future experiments (Muon g-2/EDM in JPARC). This will provide additional interesting inputs to this R&D line.

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Several members of the SiLC collaborations are members (HIP Helsinki, LPNHE Paris, Charles University Prague and IFCA Santander) or associated partners (IMB-CNM/CSIC Barcelona, IEKP Karlsruhe, NRNU-Russia, IFIC/CSIC Valencia, HEPHY-Vienna) to the EUDET, FP6 I3 E.U. project.
Several contracts between different partners of SiLC, these last years:
Contracts CICYT-MEC/IN2P3-CNRS between LPNHE, IFCA, IFIC and B.U.
Contract France-Japan: LPNHE and KEK
Contract PiCS: France Russia between LPNHE and NRNU.
Collaborative contacts with CERN (A. Honma, A. Marchioro and test beams)
Collaborative contacts with DESY (especially for the beam test infrastructures)
Collaborative contacts with B. Cooper and M. Demarteau at FNAL.
{*} Master 2 Internship.

Introduction

This status report presents the work achieved by the international R&D Collaboration, ***SiLC*** (**Si**licon tracking for the **L**inear **C**ollider), over the last two years starting in May 2008. The R&D objectives of this collaboration are centred on the developments of a new generation of Large Tracking systems based on the use of the Semi-conductor technologies. The first proposal was presented at the PRC DESY in May 2003 followed by an addendum in October 2003 [1]. A first status report was given two years later in May 2005 at the PRC-DESY [2]. The third status report to this Review committee was given on April 2008 [3], after the detailed report given by this collaboration to the Tracking session of the ILCSC R&D panel on February 2007 in Beijing during the BILC07 workshop [4].

The first remark is about some changes in terms of the collaborating Institutions with respect to the original list of participants [3]. The University of Barcelona, joined SiLC in 2008, The UK, despite funding problems, is now represented by Rutherford with the active participation of Ch. Damerell. KEK is joining with the collaboration on already starting (BELLE II) or near future (Muon g-2/EDM at JPARC) experiments. This is a real asset for both parties; it reinforces the SiLC R&D activities by offering a unique training camp, and in counterpart the SiLC contributions are instrumental to the construction of these new experiments. An opening of SiLC activities to CLIC happened over the two last years, on several aspects, namely: Front End Electronics, physics simulation and related detector performances studies.

A third main Silicon Research Laboratory has joined CNM-IMB, VTT in the SiLC collaboration, namely: IRST in Trento who joined since more than one year. These Labs are instrumental in the developments of novel Silicon sensor technologies (see Section I). The Korean participation after some downtime due in part to the sabbatical leave of H. Park is now restarting its collaboration and bringing a very valuable potential.

A second remark is to point out that, as all the R&D activities, SiLC suffers a real decrease in funding and thus in job positions. This is occurring at a time even more demanding in the LC schedule and when new experiments are interested by the contributions of the SiLC R&D.

The section I of this report presents in some details the latest advances on the three basic R&D objectives: on novel sensor technologies, on new Front-End readout Electronics and related mechanical issues. The section II describes the tools developed to achieve these R&D objectives. This includes the development of the simulation tools and the active tests programme both at the Lab test benches and test beams, at CERN-SPS and DESY. These test beam activities are closely related to the EUDET, E.U. FP6 Infrastructure Program, to which four SiLC Institutes are directly participating. All the SiLC collaborators including those from Asia and US are benefiting from the EUDET framework and give in counterpart fruitful contributions to it. The EUDET memos describing several aspects of the SiLC activities these last years are largely referred in this report.

The Section III presents the work achieved by the SiLC collaboration for the Letter of Intent of the detector concepts and especially ILD. A last section, section IV, addresses the SiLC participation to the overall LC schedule with in particular the preparation of the DBD in 2012 and the CLIC CDR in 2011. The synergies and opening of SiLC to experiments starting in the near future are briefly presented in this last section.

[1] PRC R&D 03/02 and update 01/03 in http://www.desy.de/f/prc/html/documentation.htm
[2] PRC R&D 03/02 update 02/05 in http://www.desy.de/f/prc/html/documentation.htm
[3] PRC R&D 03/02 update 04/08 in http://www.desy.de/f/prc/html/documentation.htm
[4] SiLC proposal to the ILCSC R&D Tracking panel, BILC07, Beijing Feb. 2007 in:
http://lpnhe-lc.in2p3.fr/DOCS/beijing.pdf

Section I: R&D main objectives

The SiLC collaboration is pursuing the R&D on the three main aspects: sensors, Front End readout electronics and mechanics. These three aspects are of course closely related and have as main goals to improve the detector performances in spatial and momentum resolution as well as in lowering the material budget and in still increasing the reliability and robustness of the overall system.

I-1: New sensors R&D

The SiLC R&D collaboration is benefiting from a large expertise and also good contacts with several founders or highly expert Laboratories. Some Institutes like HIP (with VTT) or Kyungpook National University (with ETRI) are in close collaborative contacts with dedicated research Laboratories or industrial firms. This also includes our KEK colleagues and their links with Hamamatsu HPK. Moreover the participation to SiLC Collaboration of highly expert Laboratories such as IMB-CNM in Barcelona or now IRST in Trento are major assets in the development of the needed novel sensor technologies.

I-1-1: The microstrips baseline

A baseline sensor design has been established to get comparable results from different sensor producers. Since future silicon strip sensors for the ILC will need a very high spatial resolution, a readout strip pitch of 50μm is foreseen, with intermediate strips in between, resulting in a 25μm effective pitch that were demonstrated to give an improved spatial resolution. The sensor bulk material is agreed to be p-on-n float zone silicon. The bulk material should be of high resistivity (5-10 kΩ cm) and rather thin the goal is to have a maximum thickness of 200μm. However, the lower limit of the thickness is limited by the noise figures of the readout chip. The detector must have a very low dark current of <1nA per strip, since the noise is mostly defined by the dark current and bias resistors.

For the inner silicon layers, we are considering two possibilities, either DC single-sided sensors as for the outer case, or AC coupled double sided detectors made on 6" wafers. For the outer layers, larger wafers of 8" or even 12" inch would be preferred to reduce the material necessary for mechanical support. In this region, the single sided detectors preferably DC coupled for cost reduction, are the considered option.

Since multiple scattering is a crucial point for high-precision ILC experiments, the amount of material inside the detector must be kept on a very low level to avoid degradation of the feasible resolution of the devices. The most radical solution is to integrate the pitch adapter completely into the sensor. The connectivity of the strips to the readout chip can be made by an extra metal layer for signal routing which is separated from the strips using an additional oxide layer. In this scenario, the readout chip can be wired or bump-bonded onto the sensor as for pixel detectors. SiLC and especially HEPHY has started to work on this solution and other solutions for direct connectivity are being considered as well (see I-2-2).

The SiLC collaboration is in contact with different sensor producers and has already started collaborating with them to produce the first prototypes according to the first step of the work program. Only vendors which are willing to collaborate and to provide sensors and test structures now are considered for the future parts of the work program.

The first batch of silicon sensors ordered at Hamamatsu Photonics (HPK) in Japan end of 2007 have been presented in the previous report as well as the complete characterisation at the Lab test bench (especially Karlsruhe and Vienna). They have been followed since then by a series of tests at the CERN-SPS (see section II).

This order consists of 30 normal sensors plus 5 "alignment sensors" with the Al backplane metallization removed in a 1 cm circle in the middle of the sensor for allowing the laser light

to pass through it (Fig. 1). This report will emphasize the series of tests performed with these 5 friendly-alignment (A.F.) sensors especially this last year. As for the 30 normal sensors, various small test structures have been placed around the main detector on the wafer, e.g. diode, MOS, gate controlled diode, and others. Four large test structures have been designed with two different purposes. Two structures comprise 256 strips with the same pitch as the main detector, but with regions of different strip widths and different intermediate strips. Each region consists of 16 individual strips with the same geometry. Both structures are used to test cross-talk and inter strip capacitances in a test setup and the resolution in a future beam test. The two other test structures on the wafer take advantage of different biasing schemes and have been designed to test FOXFET and punch-through biasing methods.

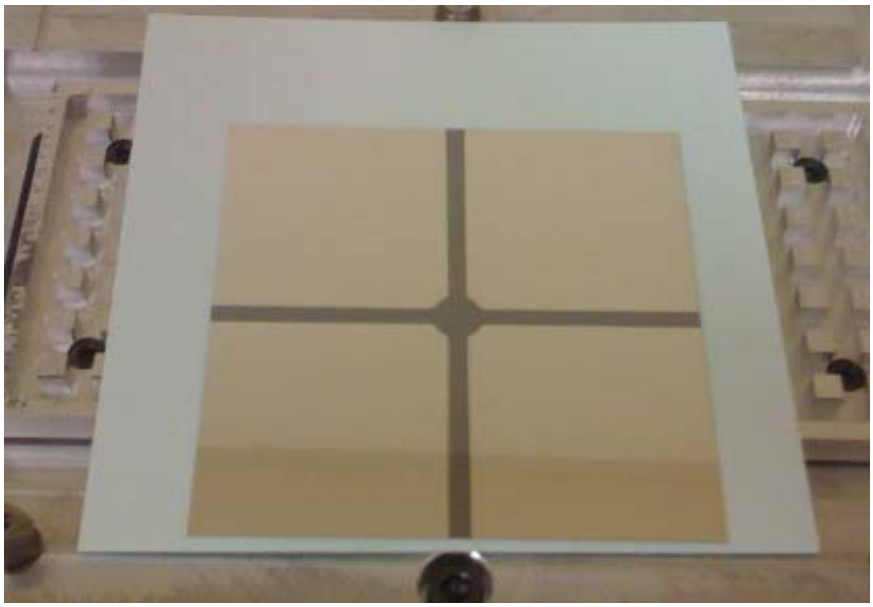


Fig 1: Photograph of one A.F. HPK sensor clearly showing the regions where the Al Back plane was removed (darker regions)

The transmittance of the HPK A.F. sensors was measured to be about 20%; an R&D is ongoing in order to get much higher transmittance Silicon sensors (see section I.1.3).
KNU in collaboration with ETRI in Korea develops new strip Silicon sensors that will be tested in test beams in 2011, and are of both types: single and double-sided, AC or DC coupled [7]. First prototypes have been electrically characterized as well as tested on test beam. The SiLC collaboration is pursuing the goal to establish companies to deliver silicon detectors for future HEP experiments.
The next goals are the development of sensors with dual metal layer structure for in-sensor routing. Together with this, a cheap, industrial bump-bonding technology must be established to take full advantage of this technique. In parallel, sensor producers will be encouraged to build doubled sided detectors, together with evaluation of companies capable of 8" inch or even larger wafers. Another line of R&D encouraged by SiLC is the development of active edge and of higher transmittance friendly-alignment strip sensors. The progress on these various aspects in these last two years is reported here below.

[5] EUDET-Memo-2007-27, *Generic Silicon Strip Detector R&D*, T.Bergauer, M.Dragicevic, S.Hänsel, M.Krammer et al., in http://www.eudet.org/e26/e28.
[6] Th. Bergauer, *Silicon Strip Sensor R&D and results from HPK sensor measurements*, presented at the Sixth SiLC Workshop in Torino, University degli Studi, Italy, Dec 2007 (http://www.silc.to.infn.it/doc/papers/) and at the TILC08 Workshop, March 2008 in Sendai,

Japon (http://www.awa.tohoku.ac.jp/TILC08/, see program)

[7] H.J.Hyun (KNU), ''Development of Silicon Strip Detectors'', presentation at the Joint Korea-France Collider Physics Workshop, 28-30 June 2010, KNU, Daegu, Korea. http://hcpl.knu.ac.kr/indico/conferenceOtherViews.py?view=standard&confId=1

I-1-2: The novel edgeless sensor technologies

The motivations for edgeless sensors are:

- They allow building large area Silicon trackers seamlessly tiled detector matrices
- No need for sensor overlap
- Decrease of the material budget
- Improvement of the tracking performances both in momentum and spatial resolution

SiLC is pursuing two R&D lines. One is based on the edgeless planar strips with active edge on n-type substrate as developed by IRST Trento.

As a last milestone in the TRIDEAS R&D INFN [8] project which also include developing 3D sensor technology, planar detectors with active edges are realized (see Fig 2). Numerical simulations are performed in order to investigate in detail the critical region of these detectors, i.e., the surface region in between the outermost junction and the active edge. Basing on the simulation results, the wafer layout was designed in fall 2008 consisting of p-on-n mainly strips. The plan was to be able to start the fabrication beginning 2009 and to complete it in 2009. Trench edging steps are investigated on test wafers. The external service is done by SINTEF for wafer bonding. First wafers were produced and electrically tested but the quality is not satisfactory especially for what concerns the trench edging. A new submission is underway and should produce better quality sensors. They are expected to be ready for the test beam in November.

The design of the wafer and the details of the connecting pads are given in the Figure 2. The sensor prototype that will go to test beam in November are the ones in the central part of the wafer and represent a total area of 2.5x5 cm^2, 50 µm pitch with floating strips. Both AC and DC pads connection are available as shown in Figure 2.

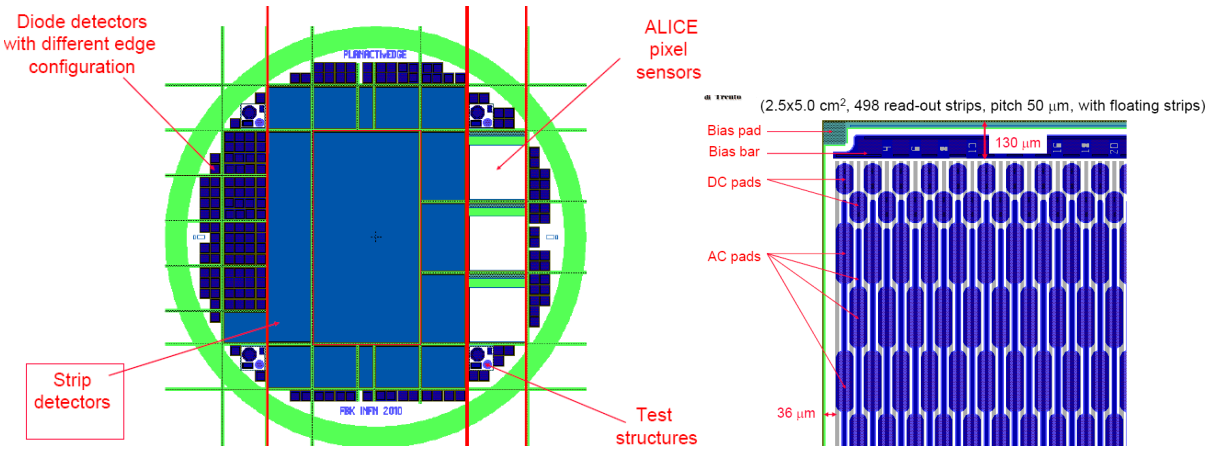


Fig 2 Layout of the planar edgeless sensors as developed by IRST Trento

Another edgeless strip sensor option follows the edgeless 6'' technology developed by VTT (*Valtion teknillinen tutkimuskeskus* in Finland). This is an alternative fabrication process that excludes all slow process steps, such as polysilicon growth, planarization and additional ICP-etching [9] and relies on a side wall ion-implantation. VTT succeeded fabricating 150 µm

thick p-on-n and n-on-n prototypes with a dead layer at the edge below 1 µm (Fig.3). The doping type at the side walls are n-type for the p-on-n and p-type for the n-on-n. The present interest is on the larger size 5 x 5 cm^2 micro-strip sensor prototypes with 50 µm pitch. Fig. 2 shows 1 x 1 cm^2 and 5 x 5 cm^2 edgeless micro-strip detectors.

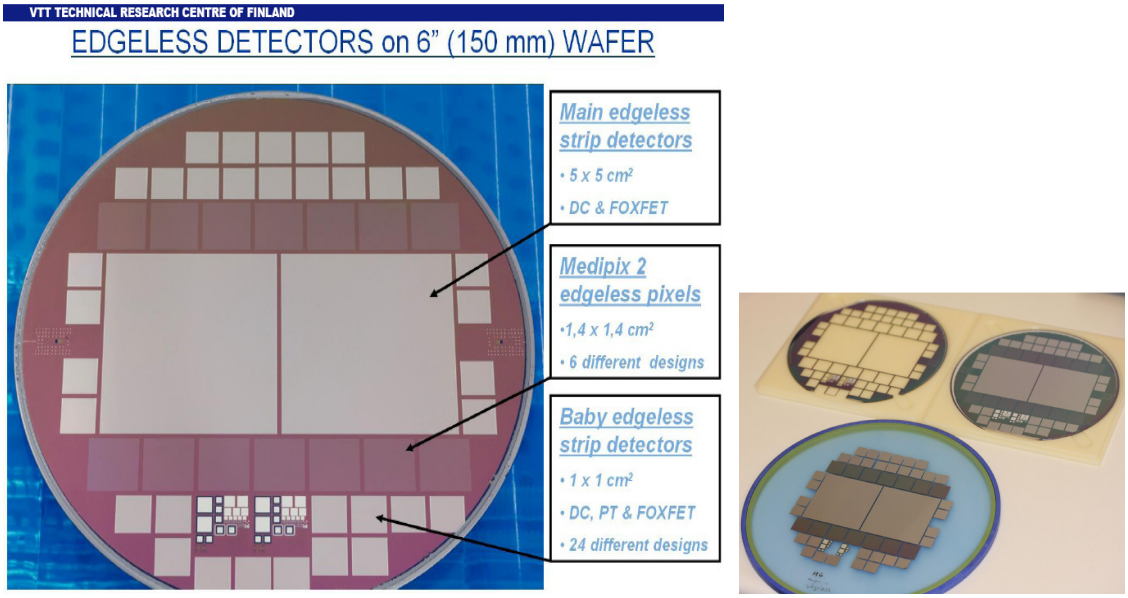


Fig 3: 6'' wafer with different edgeless strip sensors types: 5x5cm^2 and 1x1cm^2 edgeless strip sensors, with on the right view, handle wafer removal.

First electrical characterization of the strip sensors was performed by VTT on the wafer level. The breakdown and depletion voltage increase with the active edge distance. The leakage current slightly increases with the active edge distance. The capacitance increases for the p-on-n with the active edge distance. For the n-on-n the capacitance is almost independent on the edge design. Good uniformity is observed within strips.

The advantages of the n-on-n design are considered to be 1) better edge depletion (signal collection) at low voltages, 2) the possibility to collect electrons that have higher mobility than holes. Besides the electron collection is favorable in hard radiation environment but this is not crucial in the LC case where radiation hardness is not such an issue,

It is also interesting to note that the front-to-backplane depletion is 7V only for the p-on-n and 4V for the n-on-n. The full depletion of the detector active volume is 25 to 40 V for p-on-n and 13 to 25 V for n-on-n. A last but important remark is that the measured strip capacitance is about 3 to 3.5 pF/cm for p-on-n, thus only a factor 2, 2.5 worse than for the planar strips.

A new series of sensors FOXFET type (AC coupling) are under production for the test beam at CERN in November. Two first wafers were delivered beginning 2010 but with DC coupled sensors; they thus need an active pitch adapter in order to be properly connected to the FEE, thus not easy to use. But they were used for full characterization at Lab test bench and thus validated the process. The next step in SiLC will be to mount these sensors on modules and fully characterize their performances, both on Lab test bench and test beams.

I-1-3: Advances on the friendly alignment sensor technology

A large effort has been devoted these last years to develop new friendly alignment sensors. It was conducted by CNM-IMB Barcelona with the collaboration of IFCA. Both SiLC R&D and the E.U. EUDET project have been instrumental for supporting this development. The aim is the development of new infrared (IR) transparent sensors with a transmittance (T) of at least 70% (compared to 20% achieved with usual alignment friendly (AF) treated sensors) [10]. The higher the transmittance the more sensors can be aligned with a single IR laser beam.

The most complete simulation achieved in the field so far, was performed [10] in order to determine the key parameters to increase T, namely:

1. No need for a third antireflection coating (ARC): passivation layers are used as ARC.
2. Metal pitch is chosen to minimize the reflectance (10% of the pitch).
3. The thickness of the different layers is optimized to get maximal T. The outcome depends mostly on the thickness of the outermost passivation layers.

Based on these studies, new strip sensors made from 4'' wafers were produced by IMB-CNM and a preliminary set of optical tests were performed. The wafers included 12 different detectors of active area 1.2x1.5cm^2 with a circular window in the back metal of 0.5cm radius and with 256 readout strips 1.5 cm long [Fig 4.]. There are 9 guard rings and scribe line with n-well. Six detectors have floating intermediate strips, six other detectors don't. Optical test structures are added in order to characterize the optical properties of each material.

These first prototypes allow studying the impact of the intermediate strip on the optical transmittance and the characterization of T and the reflectance (R) versus the metal and/or the implant width. A spectrometer measures T of a sample in the near IR. The spectral resolution (closest two wavelengths it can resolve) is 1.2nm.

The analysis of the optical test structures shows a remarkable agreement with detailed simulation. The measured T is 70 to 80% on the optical structures. The removal of the intermediate implant does not affect R, while it gives a +20% variation in T. The metal width has higher influence on reflectance, namely $\Delta R=10\%$ between 3 and 15 μm metal width while minor effect on T, i.e.: $\Delta T<5\%$ for metal width $\geq$ 10μm. These are very promising first results.

The final aim is a technology transfer to industry for large scale production. The target to be ready for the industrial transfer is 2012, after completion of this R&D expected by end 2011.

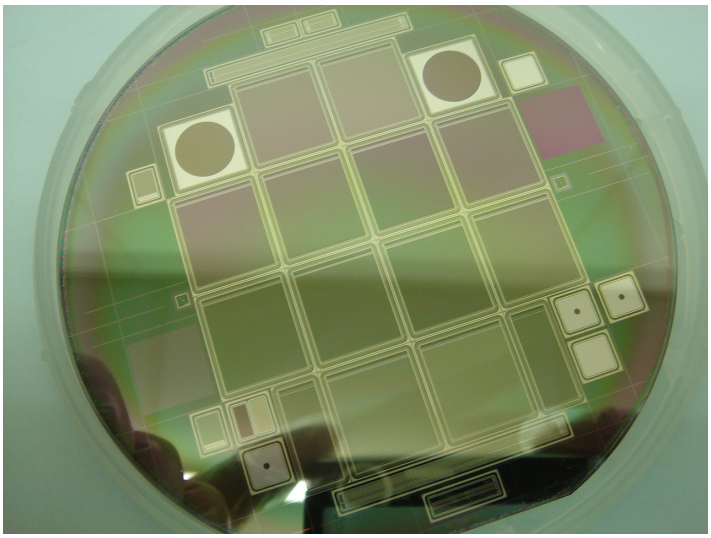


Fig 4. Photograph of the 4'' wafer with friendly alignment sensor prototypes made by CNM-IMB

[8]: Proposal to INFN Gruppo V: TRIDEAS, Development and optimization with 3D Electrodes and Active Edge, by G.F. Dalla Betta, July 2008 and references therein.
[9] J. Kallopuska et al., NIMA, 607 (2009) 85-88, and references therein.
[10] M. Fernandez et al.,"Final production of novel IR-transparent microstrip silicon sensors", EUDET Memo 2009 23, and references therein; see:
http://www.eudet.org/e26/e28/e42441/e69770/EUDET-MEMO-2009-23.pdf

I-2: Advances on the FEE and readout R&D front.

A new mix-mode analog and digital Front End (FE) chip is developed within the SiLC collaboration in deep sub micron (DSM) CMOS technology [11]. A version with 128 channels is in progress.

1.2.1 The signal processing architecture

Each channel comprises (Fig.5) *i)* a low-noise charge preamplifier with a 30mV/Minimum Ionizing Particles (MIP) gain and typical SNR of 20 to 25, *ii)* a pulse shaper operating between 0.5 and 2 microseconds peaking time (shaping time) in order to match various detectors lengths and readout conditions, and *iii)* a two dimensional structure of 8x8 analog sampler which allows storing up to eight successive events with eight samples per event. The latter is triggered by a sparsifying analog section, summing three adjacent channels from the output of the shaper. Finally, all the samples are converted by a 8-bit parallel ADC.

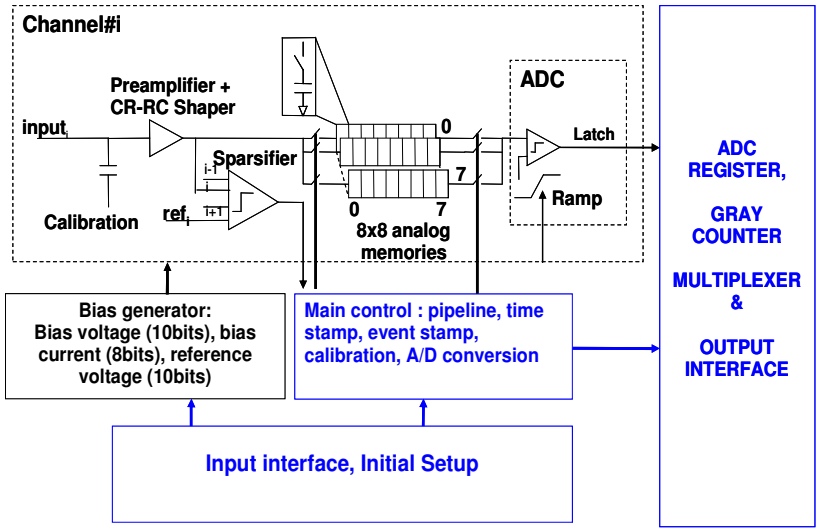


Fig.5 Channel architecture: analog and digital parts [10].

All the bias conditions of the circuit are controlled by a set of digital-to-analog converters (DAC) where the typical analog values are found in the middle of the digital range. Finally, the digitized sample is serially read out in 40-bit data words containing charge, time, channel number and event information. The static consumption of the chip is simulated at 1.1mW per channel in the active mode and 145µW per channel in the power down mode.

A first version of this ASIC in 130nm United Microelectronics Corporation (UMC) semi-conductor, SiTR_130-4 [see previous status report] was successfully designed, produced and tested at the CERN SPS [12]. It included the full analogue FE readout chain with the single ramp Wilkinson ADC. This was the baseline FE ASIC to be delivered in the E.U. EUDET project.
In mid 2008, a new version processing 88 channels was submitted to UMC semi-conductor in CMOS 130nm. It was a mix mode version, i.e. with the added digital part (elements in blue in Fig. 5) [11], and was filling 5x10mm^2 total area. The characteristics of the analog part were successfully tested and as expected [11]. See also section II on test bench results.

A new version is now underway based on 128 channels with a modular architecture, 64 channel-based. The technology is now IBM CMOS 130nm. The chip area is expected to cover a smaller total area. An updated work plan was defined in Mid March 2010, following the recommendations of an international review composed by experts on Microelectronics from CERN, Padova University and CNM-IMB. New improvements of the VFE blocks were achieved. As a result, three updated versions of the preamplifier-shaper, a new single ramp Wilkinson ADC and an updated version of the analogue memory cells were submitted to the

IBM 130nm foundry held by CERN on June 15 [13]. The VFE and readout complete chain is now under design with these improved blocks in the IBM 130nm technology.

The SiLC electronics roadmap includes:
- Going from 128 to 256 channels per chip
- Going from 128 to 256 channels per chip and/or organizing a super chip gathering several ones.
- Passing from 130nm to 90 or 65 nm CMOS technology depending what will be the most mature technology available for mixed mode ASIC.
- Thinning of the ASIC to 50 nm
- Direct connection of ASIC on strip (next sub-section)
- Developing the Data processing and full DAQ
- Adapting the FE to the CLIC cycle
- Bunch tagging at CLIC.

The last two points imply a new R&D line, just starting, in order to adapt the FEE to the challenging CLIC cycle, namely: 0.67ns bunch crossing (317ns), 311 bunches thus a total duration of 207 ns (1ms) and 20 ms (200ms) between bunch trains. A preliminary redesign of the VFE in fast mode is achieved with 20ns shaping time, low power dissipation (<300µW) and same characteristics than the ILC version in terms of noise and linearity. Power cycling option should be feasible. Work on time stamping at 10-20 ns is one of the next goals.

[11] T.H. Pham et al., "A 130nm CMOS mixed mode FE readout chip for Si strip tracking at the Future LC", Proc. of TIPP09, March 12-17, 2009, to be published in NIMA, 2010.
And
A. Savoy-Navarro et al., ''Front End Readout and DAQ for Si tracking at Linear Collider'', LCWS2010, Beijing.
http://ilcagenda.linearcollider.org/getFile.py/access?contribId=241&sessionId=13&resId=0&materialId=slides&confId=4175
[12] J.F. Genat, T.H. Pham, A. Savoy-Navarro, "Silicon Strips Detectors Readout Chip in Deep Sub Micron CMOS technology", EUDET-Memo-2007-29.
http://www.eudet.org/e26/e28/e182/e516/eudet-memo-2007-29.pdf
[13] A. Savoy-Navarro, on behalf of the SiTRA Collaboration, ''The SiTRA-JRA2 Activity: achievements and outcomes'', EUDET Annual and Final Meeting, Sept, 30, 2010, DESY: http://ilcagenda.linearcollider.org/materialDisplay.py?contribId=118&sessionId=21&materialId=slides&confId=4649

1.2.2 Direct Strip sensor and Front End connection

The aim is to develop a new module concept, all-in-one-solution, i.e. the FE chips are directly mounted onto the strip detectors. Thus no more hybrid FEE board and pitch adapter. This leads to:
- Decrease in material budget
- Simplification of the elementary module design
- And of the overall detector design
- Improved performances

The simplification of the module design implies in counterpart challenging technological developments where the cost has also to be taken into account.

The work is underway within SiLC with the following steps i) inline pitch and wiring of FE chip onto the strips [14]; ii) FE chip bump-bonded onto the strip (next step in preparation); iii) a longer term option based on 3D vertical interconnect, without excluding Tape Automated Bonding (TAB).

Vienna designed and tested a prototype built by ITE, based on step i), also proposed by SiD. Prototyped sensors from 4''wafers include 4 AC coupled sensors with 128 strips each of 80 µm pitch and different integrated pitch adapter designs and a fifth sensor with 512 shorter

strips but longer routing lines to test the influence on the SNR and the cross talk. Tests were performed at SPS-CERN in August 2009.

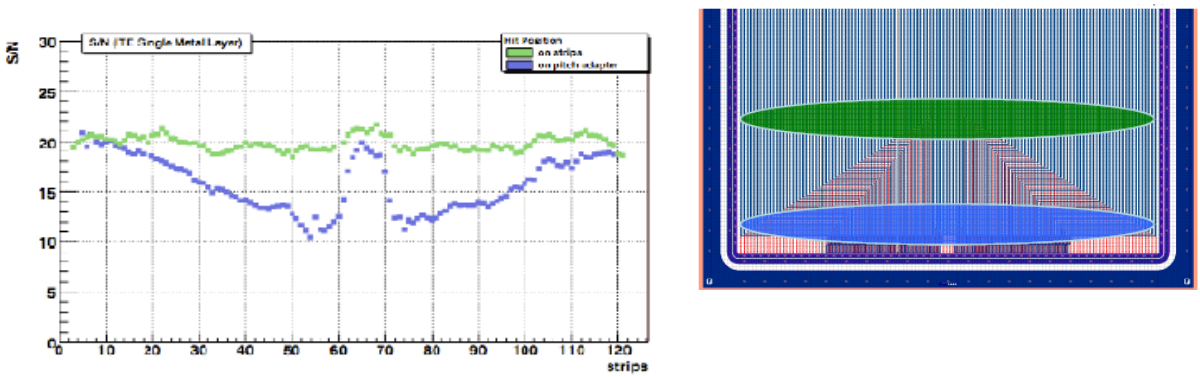
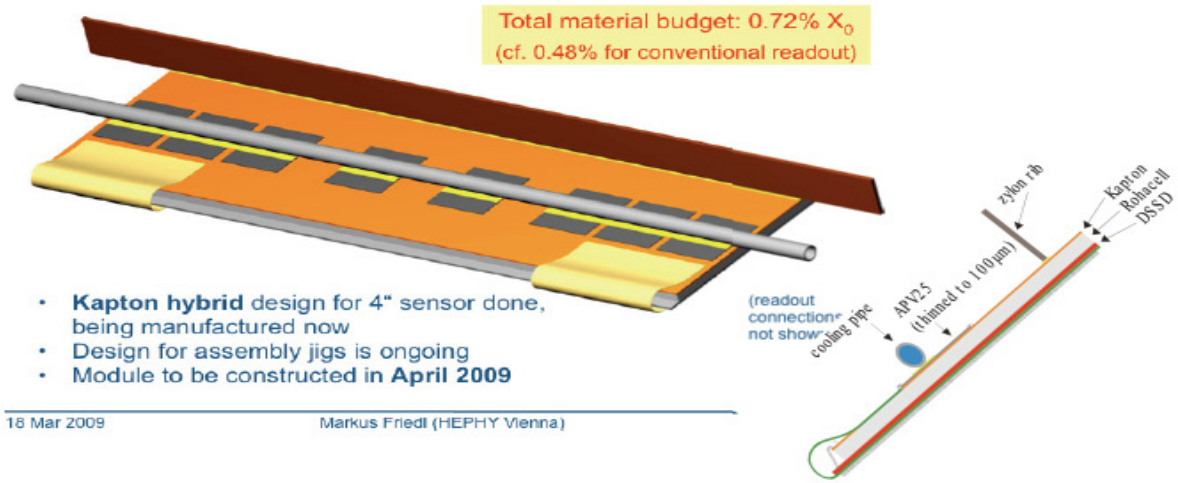


Fig.6 Signal to Noise ratio as a function of strip number thus corresponding to different wiring zones: inside (blue) or outside (green) wiring zone as shown in the left Figure.

Figure 6 shows that SNR diminishes in the routing region from 20 less than 15. This is not due to a noise increase but to a loss of signal; the capacitance of the integrated coupling capacitor gets extremely low when the metal strip moves away from implant in the routing region. The remedy is routing on a dedicated second metal layer [14].

For the 2010 test beams end of September, beginning of October at CERN the bump bonding option instead of wiring will be tested.

An alternative is under development by HEPHY and KEK and will be first applied to the BELLE II experiment at KEK. The four layers Silicon intermediate strip detector for the BELLE II experiment is being built with DSSD 6'' strip sensor newly produced by HPK. The readout chip is an adapted version of the APV25 chip from CMS. A kapton flex circuit with several APV25 chips (thinned to 50 µm) will be mounted on the DSSD sensors and both sides of the strip signal will be read out. The opposite side strips are read with folded kapton tabs (Figure 7)



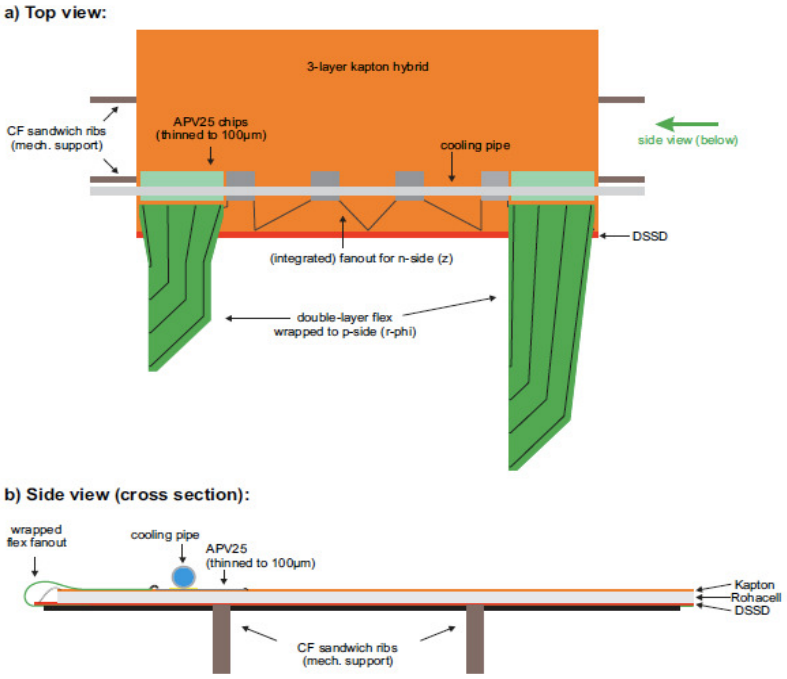


Fig.7 Schematic views of the TAB based connection developed by KEK and HEPHY Vienna for the BELLE II tracking system.

This Tape Automated Bonding (TAB) already offers a significant progress compared to the hybrid board in terms of material budget as shown in the Figure 7 above. A longer term option based on 3D vertical interconnect is also considered and will be studied within the framework of the general R&D activity in this field.

[14] T. Bergauer et al., "Silicon Strip Sensors with integrated pitch adapters", EUDET Memo 2008-18 and references therein.
http://www.eudet.org/e26/e28/e42441/

I-3: Mechanical developments

During these last two years, a large fraction of the mechanical activities was devoted to the construction of detector prototypes and of the test beam infrastructures plus a lot of work for the LOI's dedicated to the Silicon detector designs and the related integration studies. Most of these aspects will be reported in the Section II and III.
Dedicated set-ups are needed to build the Silicon modules and the Silicon prototypes. Three Labs are so far contributing to the construction of the Silicon modules and prototypes that are used in test beams since end of 2006, namely: IEKP-Karlsruhe, LPNHE-Paris and HEPHY-Vienna. Two of these Labs, i.e. Karlsruhe and Vienna had already developed expertise in building modules and Si detectors especially for the Silicon tracking system in CMS experiment for the LHC. LPNHE just started from scratch, for the SiLC R&D programme, to develop the expertise and the needed set-up for building a few Silicon modules. This subsection just summarizes the corresponding developed tools.
Two main tools were designed and built at LPNHE, namely: a tool to precisely position and align the various components of the Silicon module (sensors, pitch adapter, hybrid FE board) (Fig 8 left) and the tool to glue the sensors on a Carbon fiber support structure (Fig.8, right).

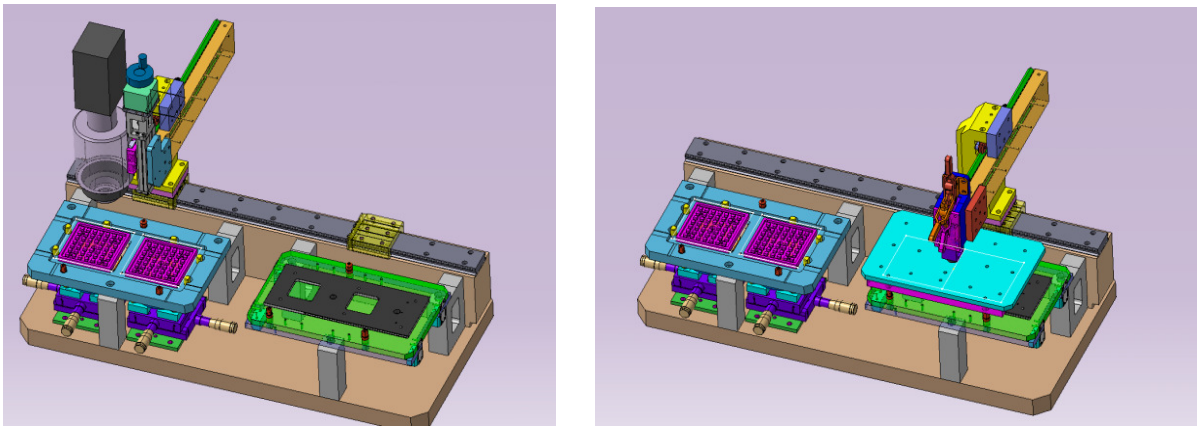
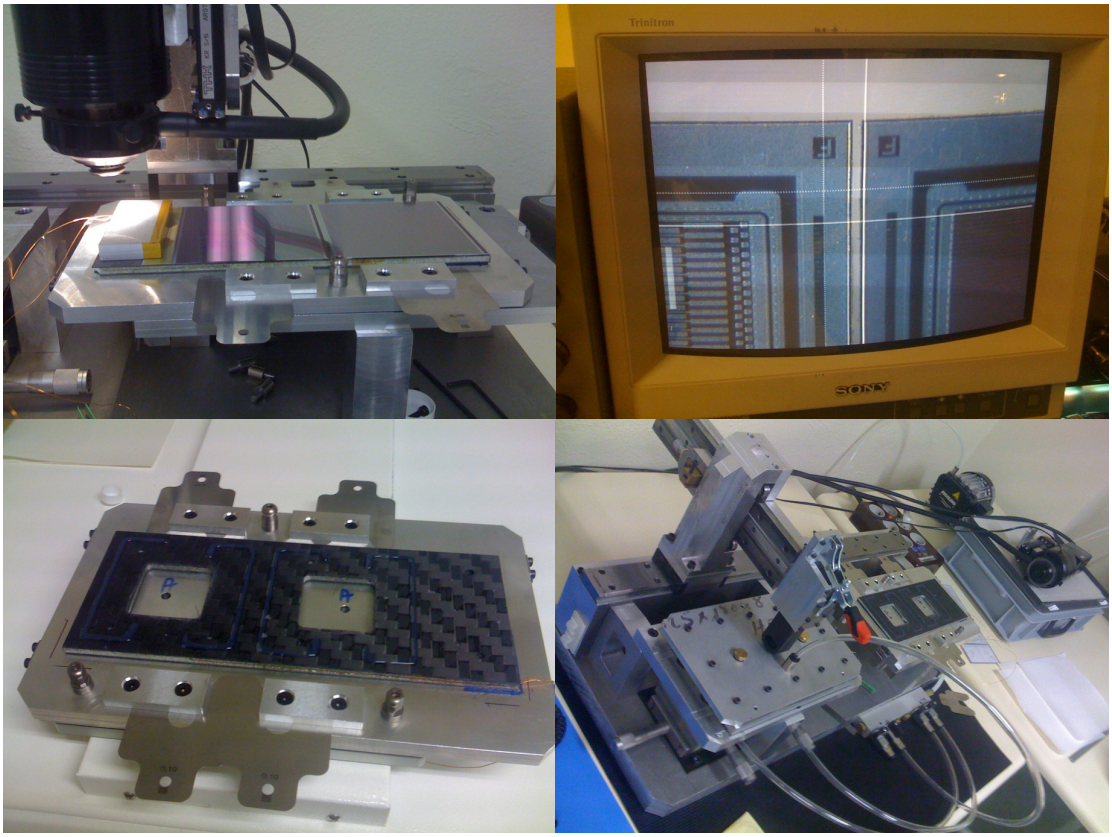


Fig 8 CATIA design of the alignment tool (left) and of the gluing tool (right) developed for building Silicon Modules at LPNHE.

The sequence to mount the Silicon modules is then as follows:

- Alignment of Silicon strips
- "Encollage" of the Carbon fiber support
- Gluing the Silicon sensors onto their support
- Positioning, alignment and gluing of the pitch adapter and FE board.

The photographs in Figure 9 show the different steps listed here above with in the last photograph the Si module in its protection box. The bonding is performed at the CERN bonding Lab.



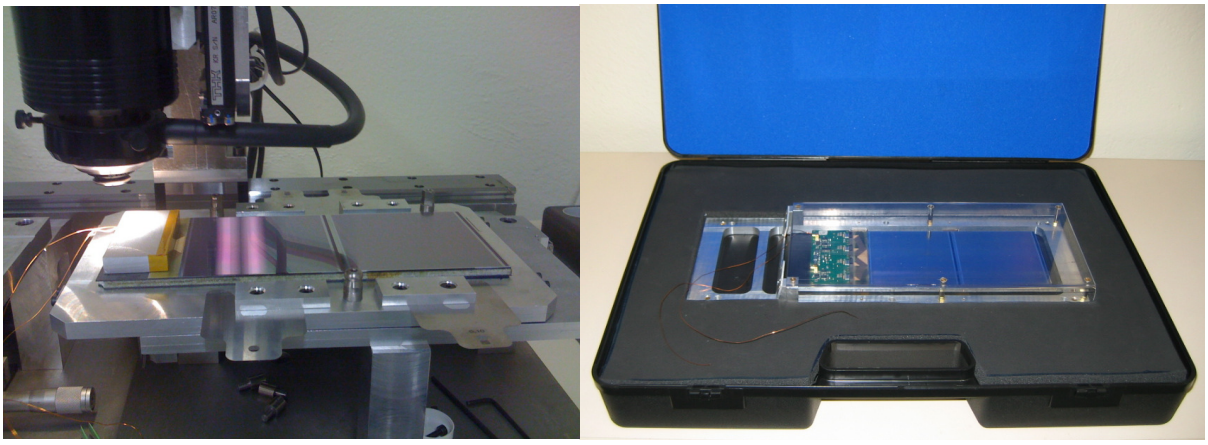


Fig 9: Six Photographs showing the different steps in the construction of a Silicon module as developed at the LPNHE Lab. Note that the bonding is performed at the CERN bonding Laboratory.

Figure 10 shows another Silicon prototype made by HEPHY Vienna. It consists of two Silicon modules installed one on top of the other with the strips of each one perpendicular to the other. The module is read out with the APV25 chip developed by the CMS LHC experiment.

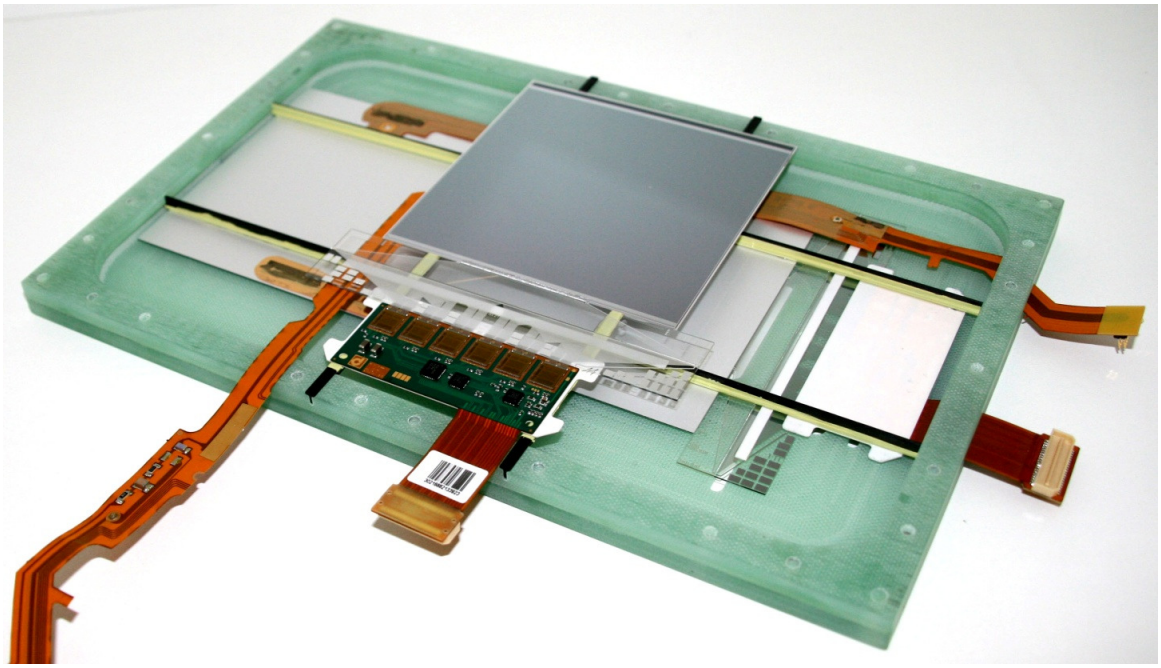


Fig. 10 Silicon modules in XY built by HEPHY-Vienna for the combined test beam LC-TPC and SiLC at DESY; this is to test the Silicon Envelope for the TPC in the ILD concept.

As we will see in the next section the capability to build Silicon modules is instrumental for the development of the overall SiLC R&D programme.

Section II: Development of tools for the R&D

Simulation tools and Lab test bench and test beams are two essential tools.

II-1 Progress on Simulation Tools

These last 2 years lot of progress was made on developing both the fast simulations and the GEANT4 based detailed simulations.

II-1.1: Fast simulations

After having used for several years the fast simulations SGV (Simulations a Grande Vitesse) developed by M. Berggren, SiLC has moved to a new tool developed by the HEPHY Vienna group, LiCToy [15]. This tool was widely used for the first step in detector performance studies for the LOI before passing to the second step i.e. the detailed simulations for a complete and refined analysis.

The "LiC Detector Toy" allows investigation of the track parameter resolution via Monte Carlo, for the purpose of optimizing a detector set-up. It features:

- Simulation of the track sensitive part of a ring or linear collider detector with a solenoid magnetic field, and its material budget;
- Support of measurements by semiconductor pixel and strip detectors, and a TPC;
- Track reconstruction by a Kalman filter, including tests of goodness of the fits.

It is written in MatLab (a language and IDE by MathWorks).

The main motivations for using this tool are:

- Comparison of track parameter resolutions of various detector set-ups, for both barrel and forward/backward regions;
- Optimization of size and position of the track sensitive devices, and of the detector material budgets;
- A simple tool – easy to understand, handle and modify;
- Easily adaptable to meet individual needs;
- Can be installed on a desktop or laptop PC;
- Quick results by "shorter than a coffee break";
- Live demonstration at a conference possible;
- An integrated graphics user interface (GUI) available;
- Ideal tool for investigating the effect of local variations.

This package provides 2D and 3D detector visualization (Figure 11)

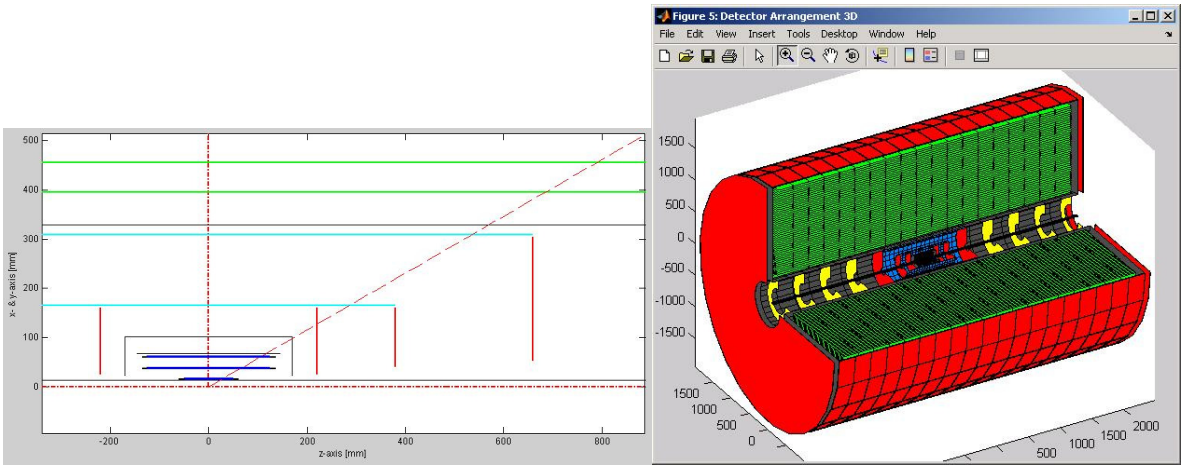


Fig. 11: 2D view of the intermediate tracking region in the ILD concept(left) and 3D view of the overall tracking system in the ILD concept (right) as produced by LiCToy.

The effect of including the SIT and the SET components in the central barrel tracking of the ILD concept is shown on the plots in Fig. 12. As an example, this Figure shows the impact of these two additional Silicon components on the r.m.s. of $\Delta p_t/p_t^2$ (left plot in Fig 1) and on the projected impact (right plot in Fig 12).

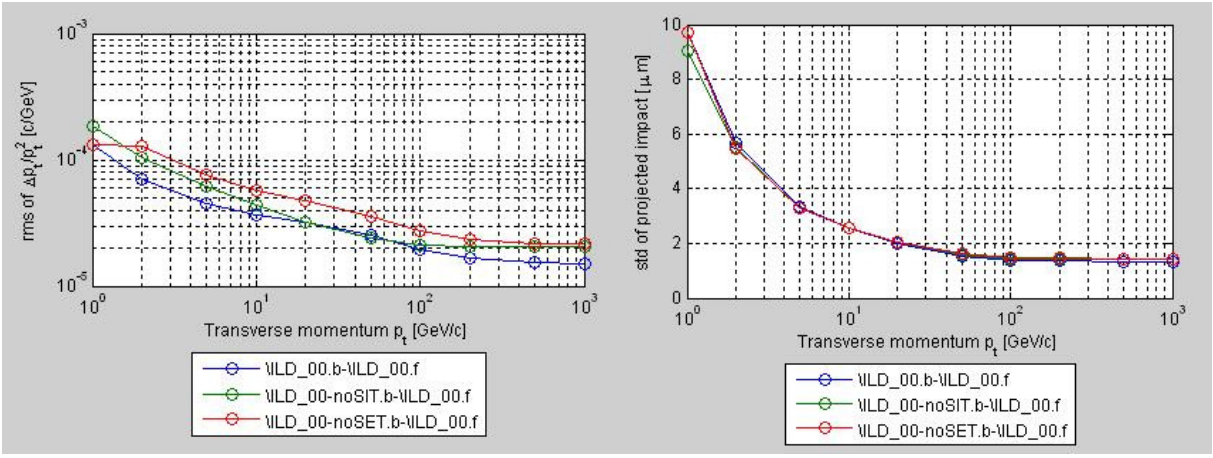


Fig. 12 Effects of including the Silicon components in the central tracking system of ILD.

This package is instrumental now for the preliminaries studies for the CLIC CDR and for preparing the ILD DBD.

[15] M. Valentan et al., ''LiC Detector Toy 2.0: tracking detector optimization with fast simulation and its application to the ILD design'', presented by W Mitaroff at the LCWS08 Workshop, Nov 16-22, 2008, Chicago
http://ilcagenda.linearcollider.org/contributionDisplay.py?contribId=217&sessionId=21&confId=2628

II-1.2: GEANT4 based detailed simulations

Two main approaches were pursued these last 2 years one based on the ILCROOT framework, the other one is based on the GEANT4 based MOKKA-MARLIN framework.
ILCROOT was mainly used for designing the details of the Silicon components in both the ILD and the SiD tracking concepts. The flexibility of this tool from the point of view of the detailed detector description permitted to establish an excellent collaborative work between the mechanical detailed design (CATIA based) and the detailed description in the simulation database of the Silicon components.
Figure 13 shows, as an example, the two Silicon detector concepts as reproduced with the ILCROOT based simulation.

SiLC is now working only in the MOKKA-MARLIN framework. The super drivers for all the Silicon components have just been defined and are being implemented in the full simulation framework. This is mandatory for pursuing the performance and Physics studies for the ILD Detector Baseline Document (Fall 2012). Two tracking concepts are made available, namely: the ILD baseline Silicon Envelope with the SIT, SET, FTD and ETD components, and a SiD like Silicon tracking. Moreover, different alternatives are included in this framework that allow comparative performances studies for the CLIC case, in view of the CLIC CDR document (Spring 2011). Some examples of the present status of this simulation framework is given in Figure 14.

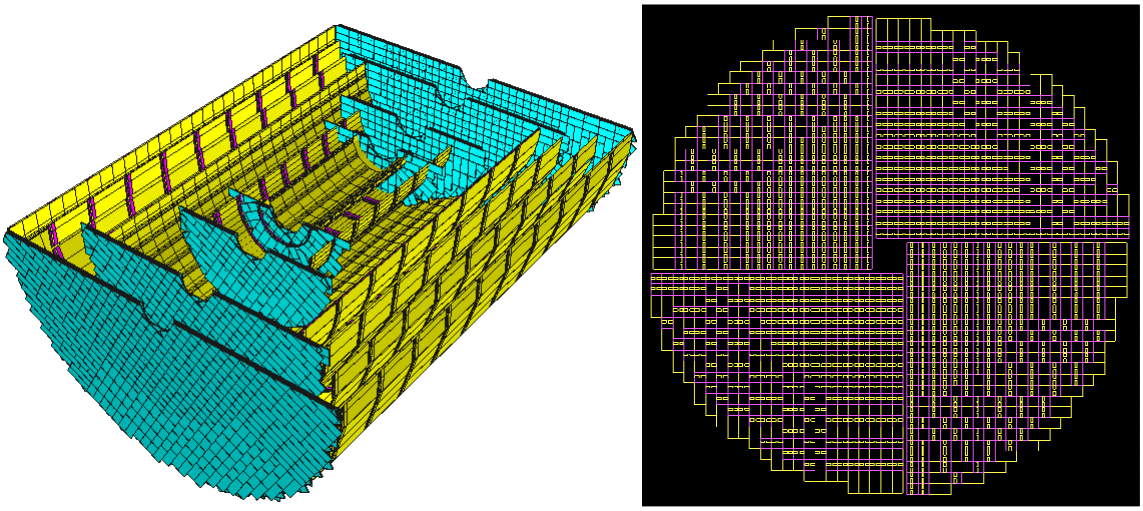


Fig.13 Detailed simulation ILCROOT based i) of the SiD Silicon tracking (left); ii) of one plan of the XUV triplet for the End Cap Silicon component in ILD concept (right).

Figure 14 shows displays from the simulation GEANT4 based in the MOKKA-MARLIN framework of the two ILC tracking concepts. The top left view shows the TPC plus Silicon components for ILD; the top right view shows the SiD Silicon tracking system.

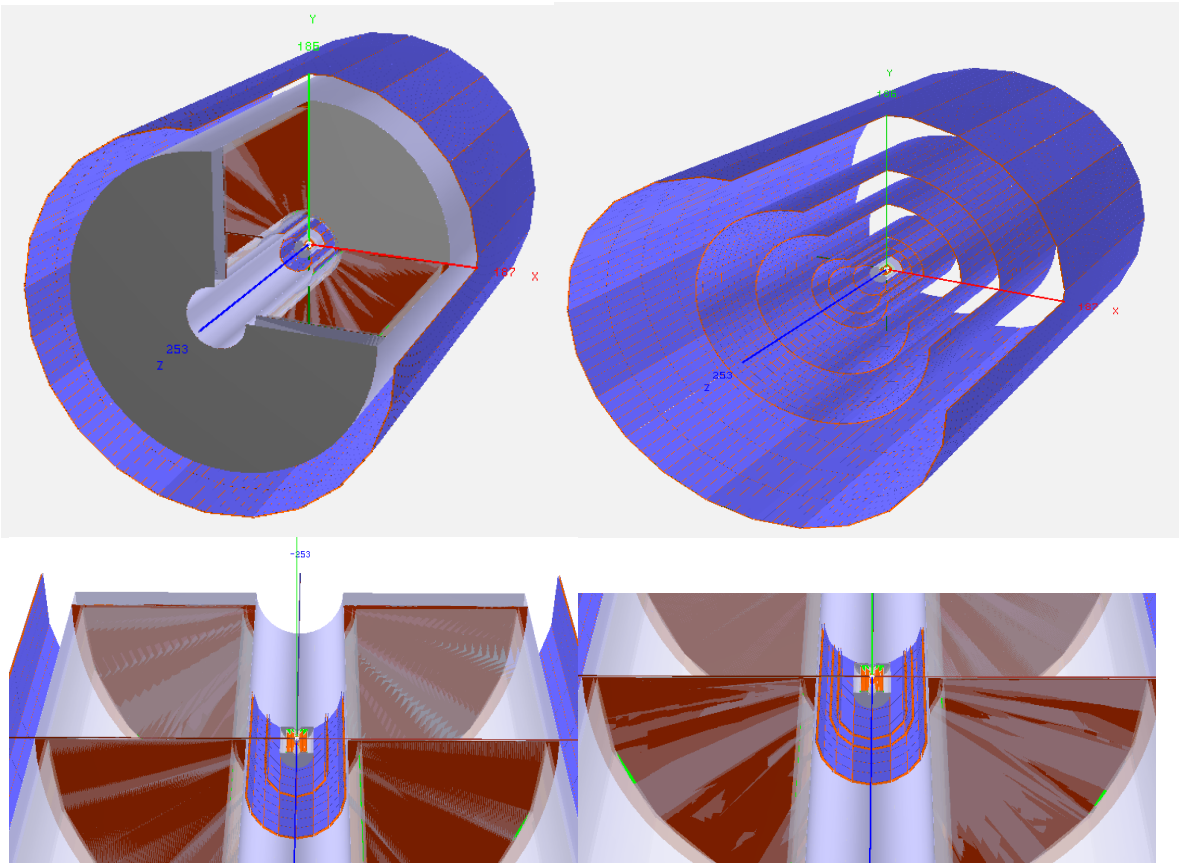


Fig. 14 GEANT4 based displays in the MOKKA-MARLIN framework of the tracking system for the ILC detector concepts (see explanation just above)

The two bottom views in Figure 14 show the details of the inner ILD tracking with two or three layers for the SIT component; this is used for instance in performance studies of the ILD concept applied to the CLIC case.
The detailed description of the Silicon tracking in the MOKKA MARLIN framework has just been achieved by the LPNHE team. This work is instrumental for the preparation of ILD DOD and CLIC CDR. Moreover it is a useful tool for any generic R&D developments.

II-2 Progress on Test bench and test beam activities

II-2.1. Test bench activities

Some new test bench facilities have been developed these last two years. This section briefly point out three of them: the optical test bench to study the development of IR transparent sensors at IFCA and the standalone and multipurpose test infrastructure developed at LPNHE also as part of the E.U. EUDET project, and the electronic test bench to test the SiTR_130 FE readout chip.
Figure 15 shows the calibration set-up mounted at IFCA to calibrate the strip sensors by comparing with an interferometric measurement leading to better than 1µm accuracy.

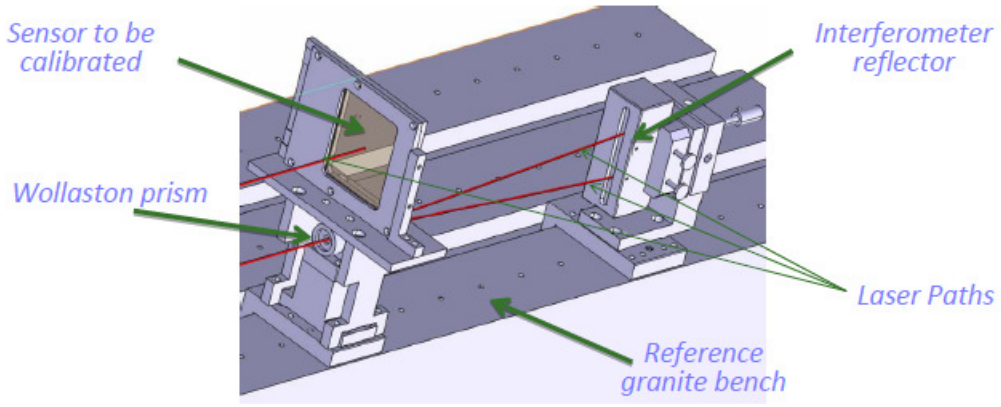


Fig. 15: Sensor calibration set-up with direct interferometric measurement (IFCA)

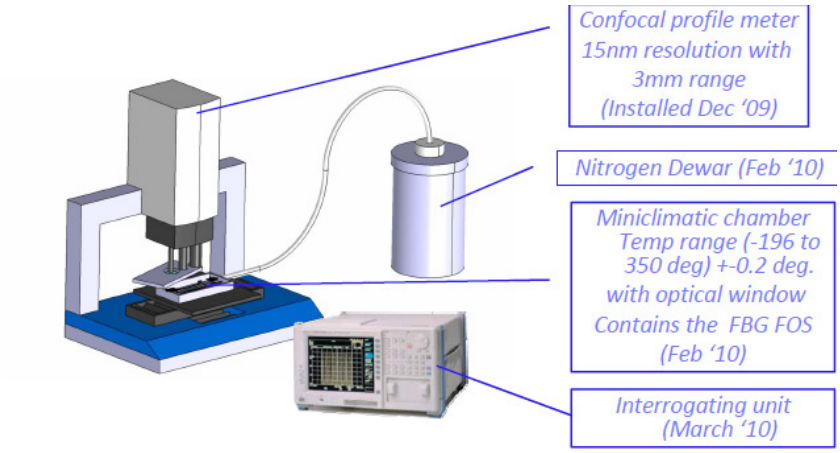


Fig. 16: Calibration of optical fibers without and with different coating (IFCA)

Figure 16 shows the set up for calibrating optical fibers without and with different coatings such as acrylate, polyimide and ormocer) [16].
Within the EUDET E.U. project has been developed by LPNHE a multipurpose and standalone test infrastructure for Silicon tracking [17]. The aim of this test infrastructure is to

test any new type of Silicon sensors (microstrips or pixels) and new prototypes of the Front End Readout electronics that process the signals from these devices (Fig. 17). A Faraday cage equipped if needed with cooling can host currently up to 5 modules with different types of sensors. On each extremity of this cage are located two modules, of false double sided type. Their sensors can be perpendicular to each other or with an adjustable stereo angle. These two false double sided modules serve as an integrated telescope in this overall test set-up (Fig. 18, right). An IR laser calibration is included in the system.

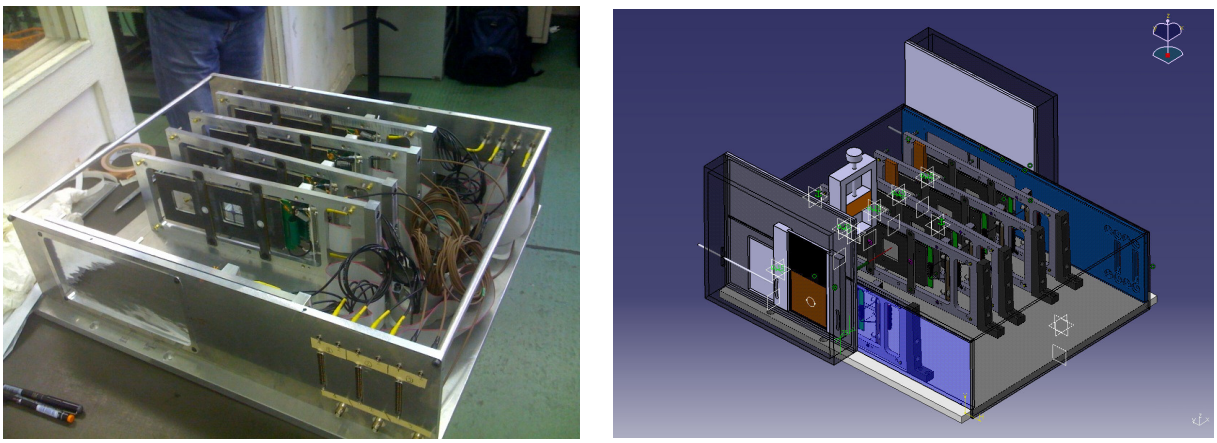


Fig. 17: Standalone multipurpose test infrastructure for Silicon tracking (LPNHE-EUDET).

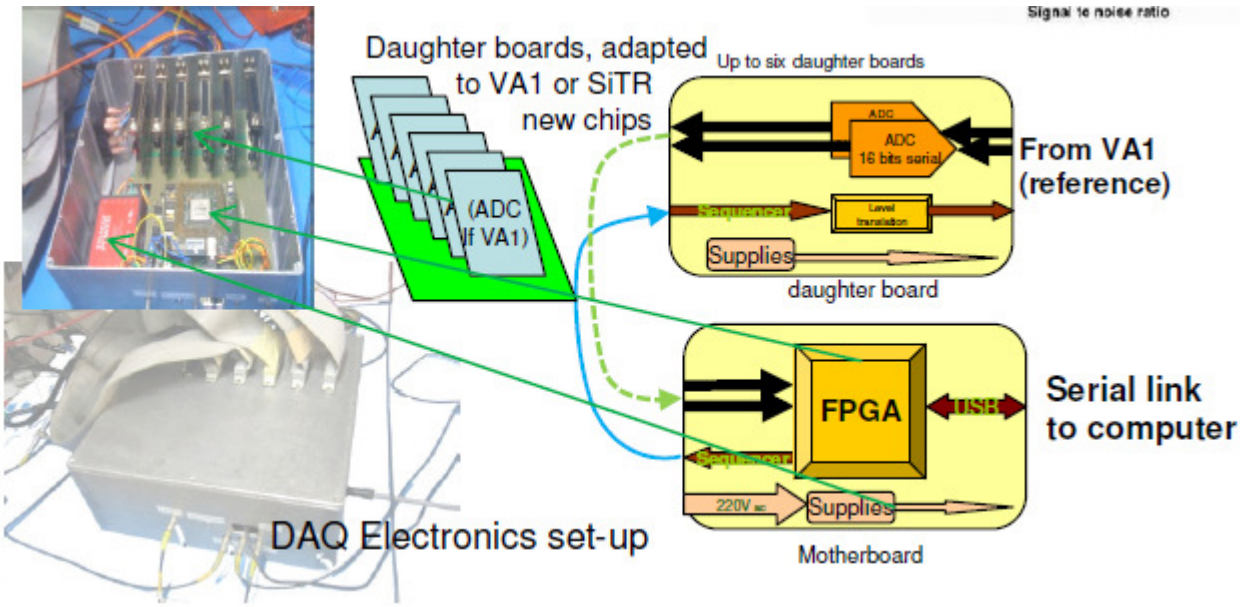


Fig. 18 DAQ for the standalone test infrastructure for Silicon tracking (LPNHE-EUDET)

The modules in the Faraday cage are equipped with hybrid boards where are sitting the Front End chips. Two types of Front End chips are used, namely: the VA1' from IDEAS, a purely

analogue device serving as reference, and the new SiTR prototypes. A completely new data acquisition (DAQ) system both hardware and software has been developed to operate this test facility.

The DAQ system (Fig. 18) includes daughter boards adapted to the type of FE readout chip. If VA1' (IDEAS) are used as FE chips, the daughter board will have to include the A/D conversion; whereas this is not the case with the new developed chip, SiTR that have the A/D conversion embedded in the chip itself. An FPGA board with serial link to the computer and USB or Ethernet connection ensures the dialog between the central DAQ unit and the electronics on detector. A complete set of monitoring, online and offline analysis packages were developed ensuring a smooth data taking with an online plots system to monitor the data taking and the functioning of the overall set-up and the analysis of data. This DAQ system is easily combined with any another DAQ system making thus possible combined test beams with other sub detectors [18].
This system was developed last year by LPNHE and used in test beam in 2010, see next section.

A dedicated electronic test bench [17] was set-up in order to test the functionalities of the SiTR_130 FE chip prototypes (Fig.20). This is an example among a few others of such test set ups developed within the SiLC collaboration such as the ones in SCIPP [19] or in KNU for instance.
The Paris test bench shown here below includes a Faraday box hosting the SiTR_130 chip prototype and an associated FPGA/USB card that ensures the dialog and test operation management through a dedicated online system operated by a VHDL/C++/ROOT based programme. A logic analyzer is used to send the signals to the FE chip. The oscilloscope allows verifying the proper functioning of the Front End; here are shown the preamplifier and shaper signals from the SiTR_130-88 prototype (Fig. 19).

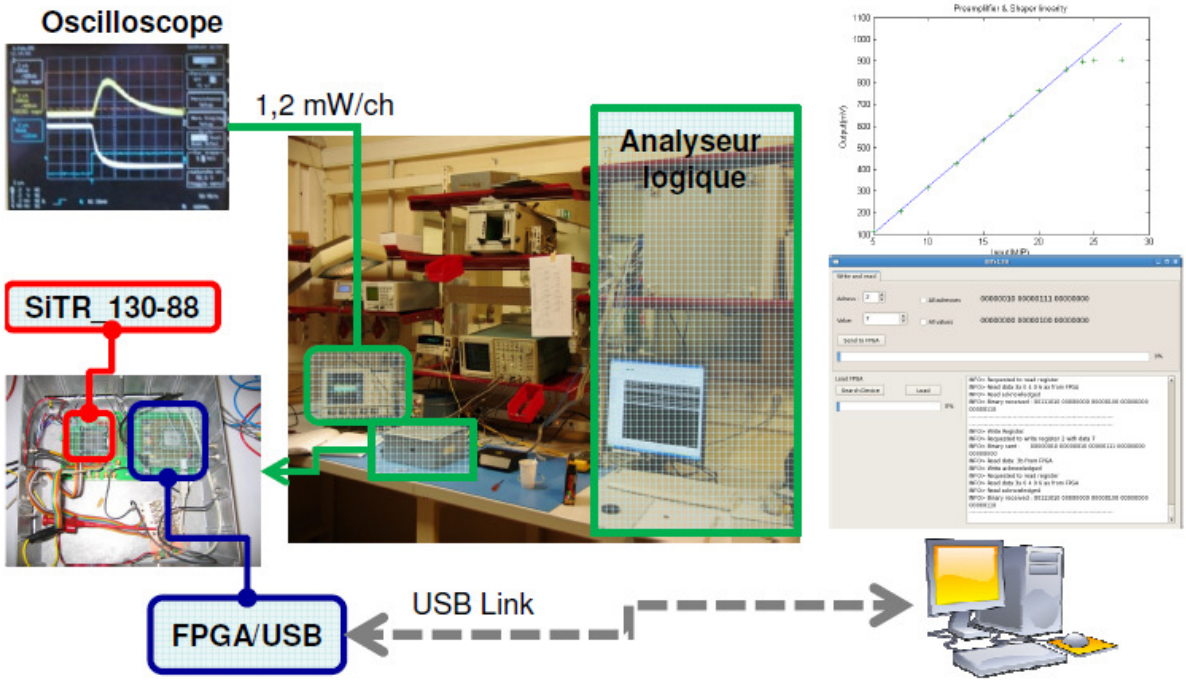


Fig.19 View of a typical electronic Lab test bench for testing the functionality of the new SiTR_130 FE chip in DSM 130 nm CMOS technology.

[16] A. Ruiz et al., ''Overview of Spanish tracking R&D for FLC'', LCWS2010, Beijing.
http://ilcagenda.linearcollider.org/contributionDisplay.py?contribId=242&sessionId=13&confId=4175
[17] A. Savoy-Navarro, on behalf of the SiTRA Collaboration, ''The SiTRA-JRA2 Activity: achievements and outcomes'', EUDET Annual and Final Meeting, Sept, 30, 2010, DESY: http://ilcagenda.linearcollider.org/materialDisplay.py?contribId=118&sessionId=21&materialId=slides&confId=4649 And,
M. Lozano et al., ''JRA2 SiTRA Silicon Tracking Infrastructure'', EUDET-Memo-2008-56
http://www.eudet.org/e26/e28/e615/e860/eudet-memo-2008-56.pdf
[18] A. Charpy, on behalf of the SiLC R&D collaboration, ''SiLC Test Beam Experience/Plans'', at the Test Beam for Linear Collider Workshop, Nov. 2009, Orsay.
http://ilcagenda.linearcollider.org/getFile.py/access?contribId=38&sessionId=21&resId=0&materialId=slides&confId=3735
[19] B. Schumm, presentation at the IXth SiLC meeting in Paris, Jan. 2010.
http://lpnhe.in2p3.fr/spip.php?rubrique127

II-2.2: test beam activities

A series of test beams are performed by the SiLC collaboration at the SPS-CERN North Area in 2008, 2009 and 2010. The EUDET E.U. project provides a useful framework. These tests request building dedicated test beam infrastructures for standalone or combined test beams. A combined test beam with the LC-TPC collaboration was launched in 2008 at DESY with first data taken in 2009. These activities are briefly summarized here below.

In 2008, 2009 and 2010, the HEPHY team is conducting a test beam program aiming to measure the performances of the test structures they requested and designed the mask for the HPK strip sensors ordered in 2007. Besides, this team is achieving an exploratory study on the direct connection of the FE Electronics onto the strip sensors. This second point is briefly summarized in Section 1 (I-2-2). The main results concerning the test of the Silicon HPK strip structures are summarized in EUDET Memos [20]

The test beam set-up at CERN-SPS is a combined test beam with the DUT from SiLC collaboration built by Vienna and the EUDET telescope. The data are analyzed by the Charles University in Prague team. A photograph of the test set-up at CERN is shown in Figure 20.

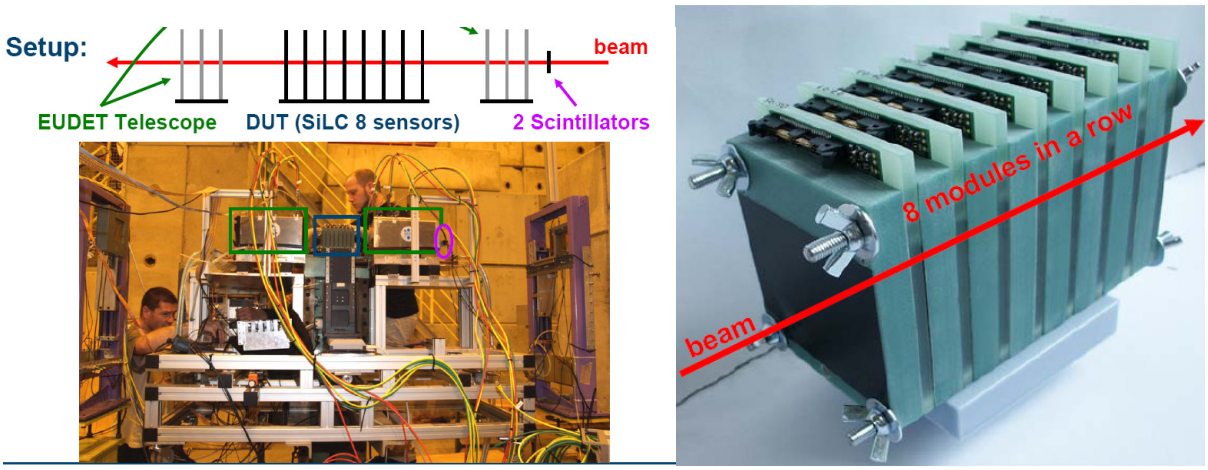


Fig. 20 Test set-up at CERN SPS with the DUT system (top right) including 8 test structures (bottom left) and combined with the EUDET telescope (top left).

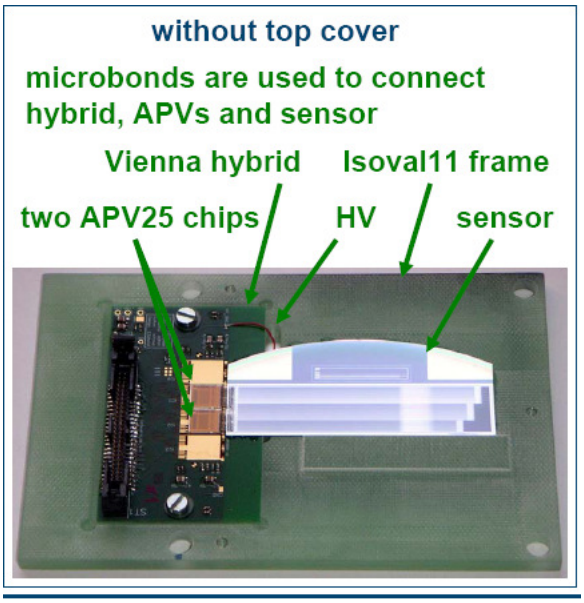


Fig. 21 (cont'd) Detailed view of one HPK test structure and the FE hybrid board equipped with APV25 chips.

The details of the test structure (Fig. 21) with different strip zones, i.e. without or with one or two intermediate strip and with different strip widths are summarized in Figure 22, left. The main result is shown in Figure 22 (right), namely: there is a significant increase of resolution for the region with one intermediate strip compared to none.
Two intermediate strips only seem to provide a small improvement compared to one strip. The achievable resolution is about 5 µm.
A slight influence of the strip width is also visible in the middle region but further investigation exploiting the full amount of data is necessary to obtain more detailed results.

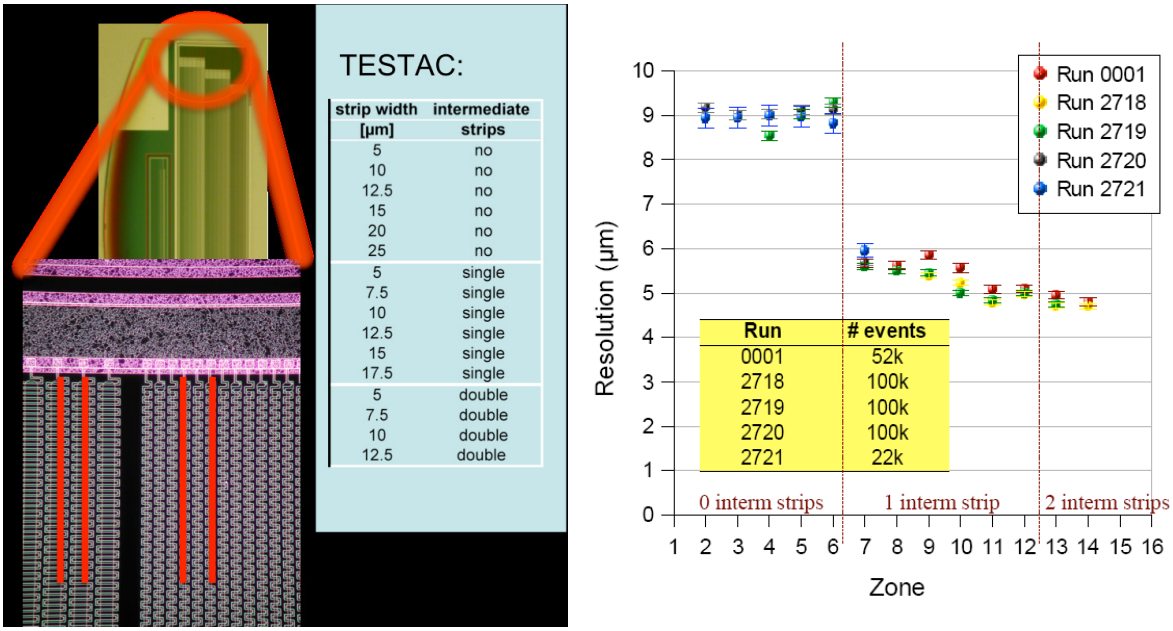
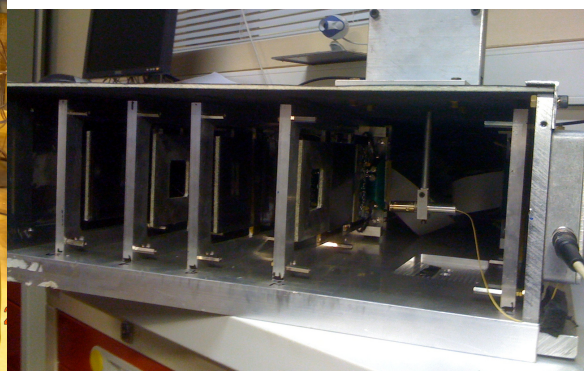


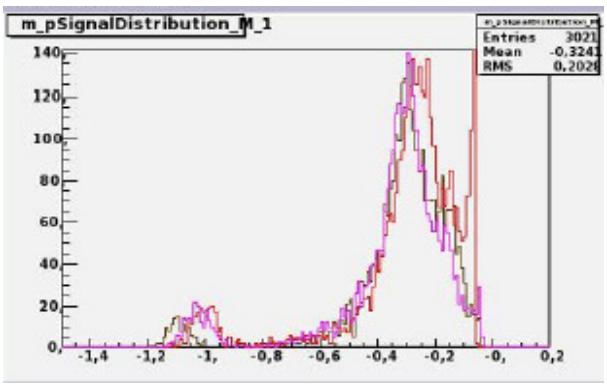
Fig.22 Details of the test structure in the HPK sensors (left) and performances in the spatial resolution as a function of the test strip zone (right)

A complete analysis package was developed by the Charles University in Prague team, within the framework of the EUDET E.U. programme [17], and used in the analysis of the data taken in this test set-up. It provides all kind of utilities with a tracking package including hit and detector alignment, tracking of straight lines, detector resolution and a validation by Geant 4 based simulations. It is used in several other test beam set-up by SiLC and also DEPFET.

[20] Th. Bergauer et al., ''Resolution studies on silicon sensors with fine pitch'', EUDET-Memo- 2008-15. See http://www.eudet.org/e26/e28/e615/e782/EUDET-Memo-2008-15.pdf

A test beam was performed in May 2010 at CERN SPS with, for the first time, the multipurpose and standalone test infrastructure briefly described in Section II-2-2, by LPNHE and Torino teams (Fig. 23).





The aim was to calibrate the new automated and very high precision table developed by Torino and to test, at the same time, this overall new test infrastructure. Another goal was to test the uniformity in response of the HPK strip sensor treated for alignment, comparing the Signal to Noise ratio along the region where the Al back plane has been removed and also in some locations where it is not remove. Many positions were scanned with beam, as shown in the schema of Fig. 24 (left). Many data corresponding to several run conditions were taken and the analysis is still undergoing.
Moreover as the set-up includes 5 layers, a preliminary track reconstruction is also experienced with this test set-up.

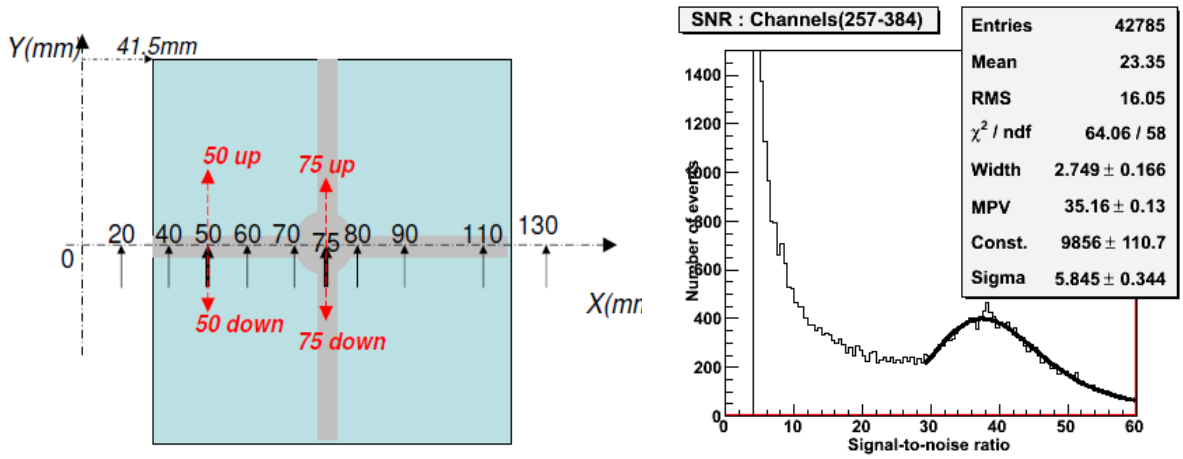


Fig. 24 Schema of the beam scan performed along the alignment friendly HPK sensor (left); Signal to Noise ratio as obtained from the off line data analysis (right)

In November a new test beam at the SPS will be performed with this same set-up but with new modules made of novel Silicon strip sensor technologies, namely the two edgeless strip sensor options previously described (Section I-1-2) from VTT and IRST and a new pixel 3D technology.

Another test set-up (Fig. 25) was installed in DESY, combined with the LC-TPC test beam set-up and took first preliminary data in November 2009 [21]. It was performed by IEKP Karlsruhe and HEPHY Vienna.

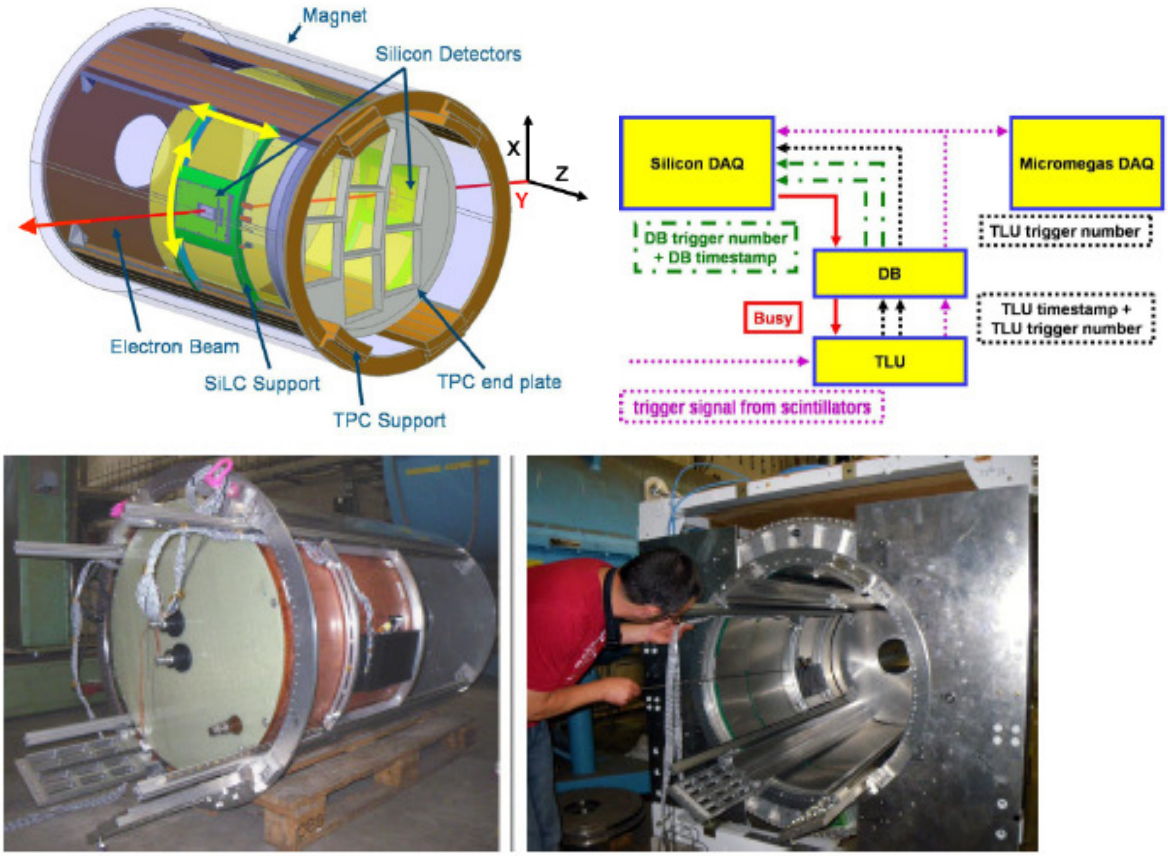


Fig. 25 Combined test beam at DESY with Silicon Envelope and Large TPC prototypes: Schema (top left), DAQ systems (top right), photographs of the set-up (bottom views).

The modules were built as shown in section I and read out with APV25 chips from CMS using a corresponding CMS based DAQ system for test bench developed and further tested with cosmics run at the Lab test bench in Karlsruhe [21]. Preliminary tests were successfully performed with the TPC equipped with the Micromegas system. Problems with the synchronisation between the Micromegas DAQ and Silicon system DAQ were mainly overcome. After this first combined test beam attempt, a new series of combined tests are foreseen in 2011 with the three GEM modules simultaneously. Moreover this combined test activity will be pursued and further developed over the next years between LC-TPC and SiLC.

[21] S. Haensel et al, ''Test Beam with Silicon Detectors around the Large TPC prototype'', EUDET-Memo-2009-17
http://www.eudet.org/e26/e28/e42441/e74986/EUDET-Memo_2009-017.pdf

Section III: Development of tracking concepts and related integration studies

Important progress towards a realistic design of the Silicon tracking concepts was achieved these last 2 years. It was largely driven by the preparation of the LOIs for the detector concepts. The letters were due on March 1st 2009 and the related activity was pursued until the end of the detector concept validation by IDAG, i.e. until end of August 2009. SiLC studied primarily the ILD concept but also gave contributions to the SiD and the 4th concept. Two tracking strategies are described in the Letters of Intent (LOI) for the ILC [22,23]. They consist in an hybrid concept, i.e. combining Gaseous plus Silicon Tracking (in the ILD case and in some sense it also was for the 4th Concept) and an all Silicon tracking as proposed by SiD.
SiLC also started under the impulse of Ch. Damerell to study an all Silicon tracking concept based on replacing the strips with pixels. The developments of these three fronts are briefly summarized here below.

III.1 The Hybrid Tracker

The ILD detector concept [22] combines a central gaseous tracker, TPC, with Silicon tracking components surrounding it, thus called the "*The Silicon Envelope*" [22]. Micro-strips are the baseline technology for building this sub-detector.
This Silicon tracking system is made of 4 components all but the very forward disks are made with a unique sensor type of 10x10 cm^2 that can be assembled into a module made of 1 or up to 5 such sensors, depending the component location. The unique sensor type is a very appealing feature of this Silicon system as it makes its fabrication much easier than the presently built large area detectors for LHC experiments (ATLAS and CMS).

The total area for this tracking system is 180 m^2, corresponding to 10^7 readout channels. SiLC R&D work is directly applied to the development of this sub-detector, including beam tests. As an example the combined test with the Large TPC prototype at DESY is a very preliminary prototype of the Silicon Envelope [21]. The integration issues are much more challenging in this case than in an all-Silicon system. Among the more difficult integration issues i) the very tight space allocated in between two sub-components; ii) the fixation and support structure on a highly constrained environment; iii) the tracking role of Si components extended to other functions, i.e. overall tracking coverage, alignment, handling TPC distortions, time stamping, entry point to calorimeters. These issues were studied in rather detailed way for the ILD LOI [22]. More work is still undergoing in preparation for the Detector Baseline Design (DBD) due in Fall 2012.
Detailed CAD design CATIA based have been produced for the various components of the Silicon Envelope that surrounds the TPC central tracker. The summary of this system is given in Figure 26.

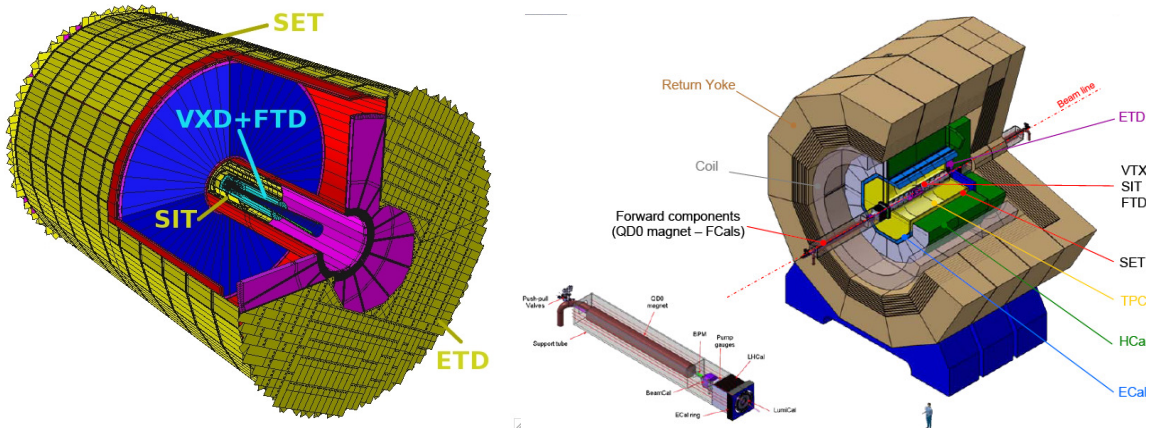


Fig. 26 *A GEANT4 based view of the overall Silicon Envelope in the ILD detector concept (left) and the overall CATIA design of the ILD detector concept.*

The number of modules for each component, the number of sensors per module and the total area per layer for each Silicon component except the very forward disks, i.e. the FTD component, are summarized in Table 1

Component	Layer #	# modules	# sensors/ module	# channels	Total surface m2
SIT1	1st layer	33	3	66.000	0.9
	2nd layer	99	1	198.000	0.9
SIT2	1st layer	90	3	180.000	2.7
	2nd layer	270	1	540.000	2.7
SET	1st layer	1260	5	2.520.000	55.2
	2nd layer	1260	5	2.520.000	55.2
ETD_F	X or U or V	82/quad =328/layer =984/ETD	2 or 3 or possibly 4	2.000.000	30
ETD_B	idem	idem	idem	idem	30

Table 1: The Silicon Envelope in numbers, for each components apart from the FTD (very forward disks) component.

The integration of a combined tracking system including both gaseous and Silicon components is quite challenging from many points of view [24].

As an example of integration study let's first discuss the Silicon External Tracker (SET) case. This device is hosted between the TPC and the electromagnetic calorimeter. It is a very large area Si component, very challenging to build because of the restricted room allocated to

it, namely 2 to 4 cm, and the fact that its support structure must be as much independent as possible of the calorimeter and the TPC. A detailed study conducted by the Torino team is underway. The first results are shown in the Figure 27. The best design was found to be a SET made of two half of 2.4 m long each and including 24 rectangular sectors (0.5m x 2.4m each). A 3 point fixation of the SET onto the TPC cage is one of the two possible fixation considered for the present time. The other proposed option is to fix the SET on the two edges of the TPC on an independent wheel and only one fixation point on the central part of the TPC.

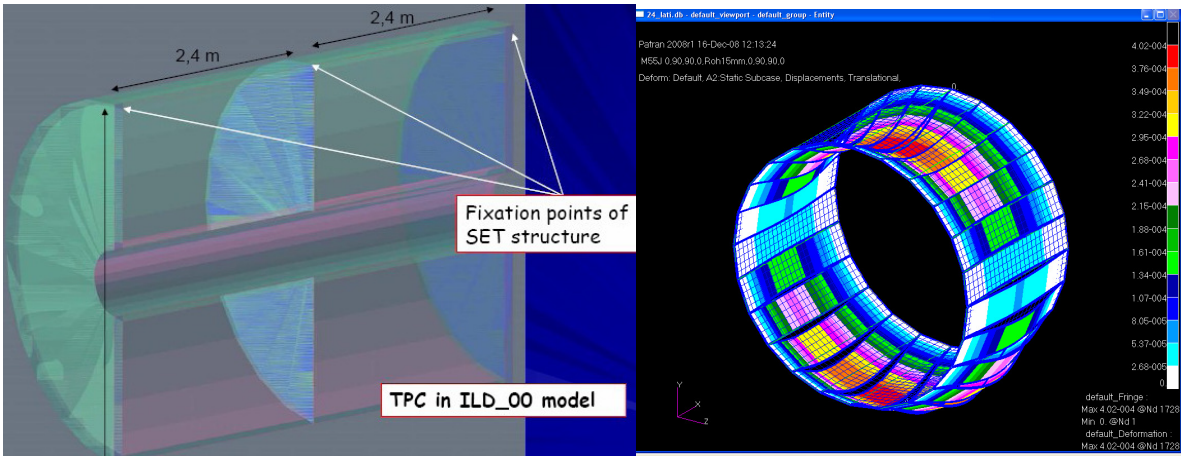


Fig. 27 Design of the SET detector into 2 half components of 2.4 m length and made of 24 rectangular sectors (0.5m x 2.4 m each) (left). Mechanical deformation map (right).

The overall support structure is defined in details and the mechanical deformation is studied and shows to give a maximum deformation of 0.4mm in the central part (Fig.27)

[22] The International Large Detector LOI, by the ILD Concept Group, Feb. 2010, DESY 2009-87, FERMILAB-PUB-09-682-E, KEK Report 2009-6.
[23] The Silicon Detector Concept LOI, by the SiD Concept Group, March 31, 2009.
[24] A. Savoy-Navarro (LPNHE) '' Integrating Silicon Tracking in the ILC detector concepts: solutions and challenges''
http://ilcagenda.linearcollider.org/getFile.py/access?contribId=126&sessionId=26&resId=1&materialId=slides&confId=3154

III.2 The Silicon Tracking Concept

Several SiLC partners are co-authors of the SiD LOI [23] and have been actively involved in developing this concept especially the all Silicon tracking system. UCSC and SCIPP are working on the development and test of the front end electronics (KPIX and a TOT alternative version) and also on a possibility of long ladder. The Ann Arbor team worked out a very precise alignment system based on interferometry measurements. The Alignment system developed by CNM and IFCA is as well included in this LOI.
More generally the SiLC collaboration is interested in the all Silicon tracking alternative and is studying the application of all the R&D aspects developed by this collaboration to this Silicon tracking case. Moreover, as already mentioned in the section on simulation studies, the case of an all-Silicon tracking is considered and embedded in the geometry DB description as an option. This ongoing activity is studying possible updates of the Si tracking system currently proposed by SiD.

III.3 The Silicon Pixel Concept

Another option for Silicon tracking at the future Linear Collider, and in particular to an all-Silicon tracking system based on strip sensors has started to be addressed by the SiLC collaboration. It consists in replacing the strips by pixels as promoted by Ch Damerell [25].
A uniform approach to tracking all the way down to the polar angle cutoff of ~7^o characterizes this tracking concept. Concentric layers (barrel plus end-plates) of silicon pixel detectors are likely to deliver a minimal material budget. Indeed the information provided by a single layer of pixels (unambiguous space points) is much greater than even two orthogonal strip layers.
In order to exclude out-of-time tracks, single-bunch timing is desirable. While one certainly needs accurate timing information for every track, such information is *by no means* required for every point on the track. Since precision timing costs power, and hence increases the layer thickness, this suggests a *'separated function'* tracking system, with the thinnest possible 'tracking layers' on the inside, surrounded by an external envelope of a few 'timing layers'. A promising layout appears to be approximately 5 tracking layers starting just beyond the vertex detector, followed by just 2 closely spaced timing layers immediately in front of the electromagnetic calorimeter.
For the tracking layers, charge-coupled CMOS pixels are suggested [25]. This advance, effectively a marriage between CCDs and simple CMOS pixels (originally developed for the high-end photography market), provides inexpensive monolithic pixel imaging devices with unprecedented noise performance, independent of pixel size. The application (the ISIS approach) for tracking has been discussed in [25]. The pixel unit cell (Fig.28) with pixels of ~50μm delivers the precision needed for a large tracking system.

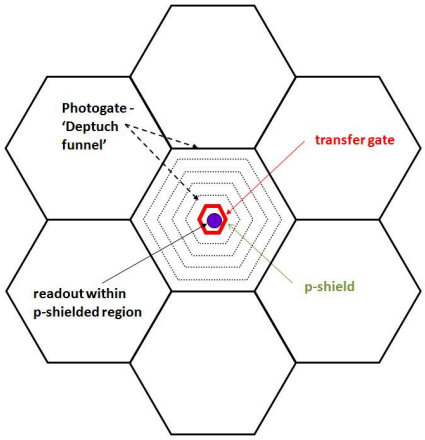


Fig.28 Suggested pixel unit cell (~50 μm diameter)

Using a charge-collecting buried channel photo-gate structure (PG) with a depleted epitaxial layer allows efficient collection of the minimum ionizing particle signal charge to the compact ring-shaped transfer gate (TG). The signal charge is held there while the current in the very compact source follower transistor is measured, followed promptly by measuring the difference due to the transfer of the signal charge from TG to the output node.
The overall tracking layers comprise ~11000 devices of size ~8x8 cm. Signals are accumulated through the bunch train and read out in the long intervals between trains avoiding the need for 'pulsed power'. The power (a few hundred watts total) is delivered continuously, so there is no issue of Lorentz forces as high currents are switched in the solenoid field. Using on-chip sparsification, the data from the complete system, can be

comfortably transferred out of the detector on one or two optical fibres at each end. From preliminary studies, a total thickness per layer of 0.6% X_0 will be achievable.

For the timing layers, hybrid pixels are envisaged, with larger pixel size (~150 μm). In this less critical region (in terms of photon conversions) a layer thickness for a liquid-cooled system of 2% X_0 is affordable. In the forward region, hit densities are considerably higher, and thus three timing layers are suggested for redundancy, so as to guarantee a mini-vector even when one of the layer hits is missing.

The overall scale of the proposed system (~30 Giga-pixels for both tracking and timing layers) is in line with 2020-trends in astronomy and the material budget (~3% X0 for tracking layers and 4-6% for the timing layers) appears to very well satisfy the LC goals.

SiLC will develop this concept under the guidance of Ch Damerell who is leading this effort and join the SiLC collaboration. While pursuing the currently developed project, SiLC will also work on an alternative pixel technology and detailed simulations.

[25] C. Damerell, et al., Nucl. Instr. and Meth. A (2010), doi:10.1016/j.nima.2010.04.154 and references therein.

Section IV: Developing synergies and outcomes

The synergy with the LHC construction and upgrades has been advertised since the very beginning of this R&D project. Indeed even if there are some aspects where both LHC and the Linear collider options are differing such as in particular:

- Contrary to the LHC, radiation hardness is not a major issue for the Linear Collider. This implies:
- The possibility to work at room temperature and with a temperature gradient $\Delta T = \pm 5°$.
- Long shaping time (typically 1 to 3 μs).
- Relatively long strips (typically 10 to 30 cm)
- Electrical power cycling is feasible and included to avoid as much as possible heavy cooling system

Moreover specific aspects of the LC machine such as:

- Only one interaction region and two detectors running alternatively impose a push-pull scenario with severe constraints on alignment for instance.
- Time stamping is requested because no triggered system but could be of interest even at LHC.

It imposes some specific constraints but all in all many issues are of common interest for both cases. It is also interesting to note as we will see in the next two sub-sections that CLIC has even more similar aspects to LHC because of its fast machine cycle.

But the new interesting aspects that have been developed these last 2 years by the SiLC collaboration is the participation to the CLIC R&D effort and the collaboration with new experiments such as BELLE II at KEK and g-2/EDM project at JPARC-KEK that are expected to start in a much nearer future as compared to LC or LHC upgrades.

IV-1: Outcomes from EUDET E.U: Transnational activities

A series of transnational activities, outcomes of the EUDET test beam infrastructures development are being developed this last year. There are 4 such applications [17].

IV-1-1: Two applications of the standalone and multipurpose test beam infrastructure for the test of the new sensors in the May and November test beams at CERN. These applications have been briefly discussed in the sub-sections I-1.2 and II-2-2 and will result in publications.

IV-1-2: Application of the test beam infrastructure for pursuing the development on the direct connection of the FEE onto the strips. This is also reported in I-2-2 and II-2-2 and will be described in a forthcoming publication.

IV-1-3: Application to the TileCal cosmic tests at CERN.
The Prague team in the Tile Cal hadronic calorimeter of ATLAS has proposed to use the SiTRA standalone test infrastructure starting in November this year and over the next years.

In order to study the calorimeter performance a spare module, identical with those installed in the ATLAS experimental hall, has been equipped with standard ATLAS readout and several long-terms tests are being performed in a surface laboratory at CERN.
Cosmic muons are triggered by the set of large-size scintillators (Fig.29). Two scintillators are stacked in the top of the module and their signal is used in a coincidence with a signal of one of the two scintillators placed side-by-side in the bottom of the Tilecal barrel module. This trigger signal is used as a ATLAS Level-1 accept, causing the standard digitized signal is read out from the calorimeter module.
The main motivation is to study the cosmic muon response using rather precise information of the muon track passing through the calorimeter.

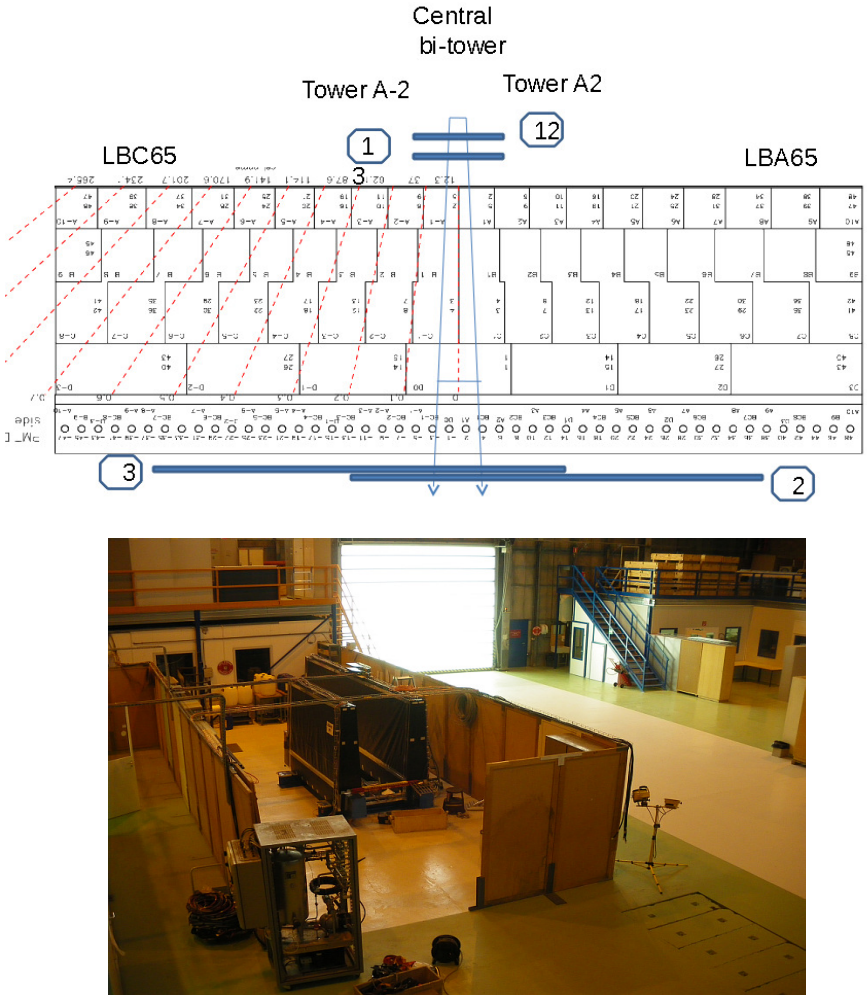


Fig. 29 Schematic view of the cosmic test with one module of the TileCal calorimeter (top) and photograph of the experimental hall at CERN where this test set-up is installed (bottom)

The current setup cannot provide information on the position of the incident particle. The only information available (independent from the tested calorimeter module) comes from the scintillators used to trigger the system. They provide no spatial information. This tracking information is expected to be delivered by the Si-strip detector [26].
The response can then be compared to the test beam results (where tracking information was provided by the beam chambers) and to that of cosmic muons in the full ATLAS setup. Studies will focus especially on the inter-calibration of the Tilecal radial layers and associated systematics.
This test session will be instrumental for deeper understanding of Tile calorimeter performance. From the response to cosmic muons one will be able to calibrate individual readout cells and Tilecal radial layers and to assess the detector aging effects. The precise positioning information, not available at the current setup version will be very helpful in proper assignment of the response to the hit part of the detector.

[26] S. Nemecek et al., ''Proposal for the usage of the EUDET TA2 Si-STRIP infrastructure at CERN from the ATLAS TileCal collaboration'', submitted to the EUDET Collaboration, Sept 10, 2010, and references therein.

IV-2: Outcomes for near future experiments: Belle II and g-2/EDM

Since 2008, several members of SiLC have launched an active participation to the BELLE II experiment at KEK. It includes HEPHY Vienna, IEKP Karlsruhe, CU Prague and some R&D contribution from IFCA-Santander. Their goal is to build the 4 layers intermediate Silicon tracker sitting right after the vertex detector. The SiLC members of BELLE II have a leading role in constructing this Si tracking component. The SiLC R&D provides new developments as well as test beam related activities very useful to this experiment (see subsection III). The major contributions include i) the new DSSD sensors from Hamamatsu HPK, tested at CERN SPS test bench in 2010, ii) the new direct connection of TAB type (see I-2-2), with thinning of the FE ASIC, iii) alignment system and iv) the test beam set-up and tests.
The outcome for SiLC is that finally HPK was convinced to start a new foundry chain for DSSD with 6'' wafers in 2009; they are being tested at the CERN SPS test beam by SiLC.

Similarly one team from SiLC, LPNHE, was approached end of last year by the g-2/EDM project at JPARC [27]. This new experiment is expected to start in 2014/2015. Their main interest is primarily in the FEE electronics and also on the test beam infrastructure and the alignment system. Adapting the SiLC developed FEE ASIC for this experiment is indeed quite appealing and very promising for future applications.

As shown in Figure 30, the muon beam cycle for the g-2 experiment has a time sequence which is quite similar to the CLIC cycle. Therefore the interest of adapting the SiTR FEE design for the g-2 JPARC case has several potential outcomes.

[27] ***Workshop on ''Muon g-2 and EDM in the LHC era'', organized by N. Saito and A. Savoy-Navarro, Paris, Feb 26, 2010,*** *sponsored by the Federation de recherchesInteraction Fondamentale*; See http://www.lpthe.jussieu.fr/fed/E_Conf.html

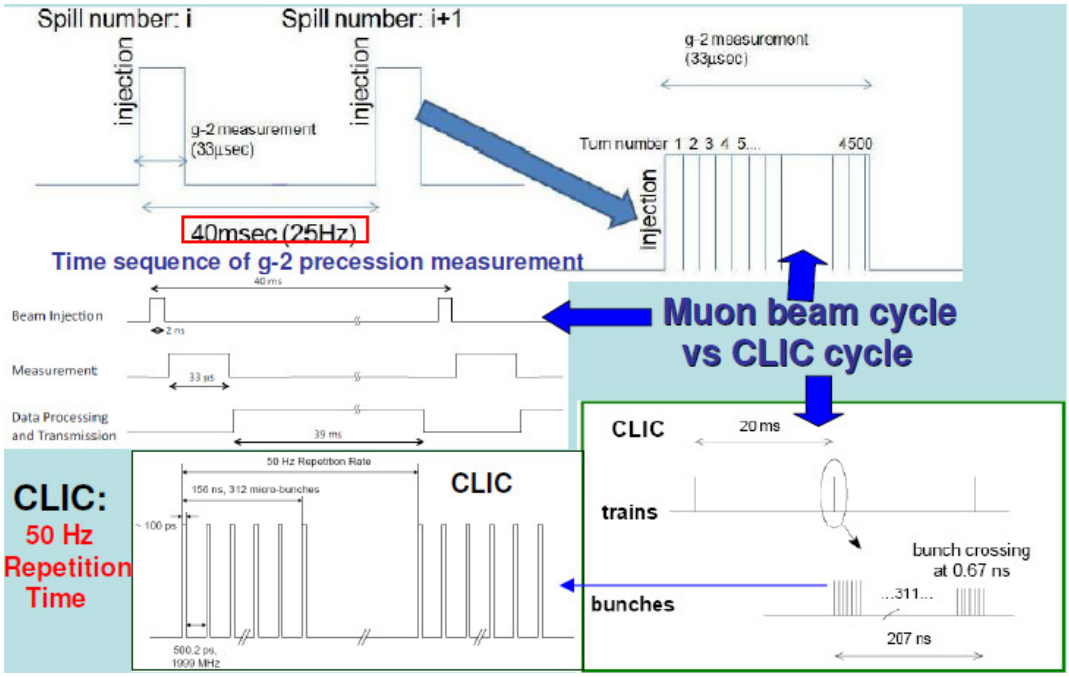


Fig.30 Sketch of the muon beam cycle for the g-2 experiment compared with the CLIC machine cycle.

CONCLUDING REMARKS

An impressive work was achieved in these last two years and is currently strongly pursued by the SiLC collaboration. It covers all the facets of this R&D, i.e.: new sensors developments (especially edgeless and alignment friendly options), new FEE electronics and the direct connection of FEE chip with the strips, tackling some related mechanical issues. This is done together with performing a series of test beams (several test beam sessions per year) allowing real life tests at each step of the developed R&D. Complete test infrastructures including Silicon system prototypes with dedicated FEE readout and DAQ system are developed and run sometime in combined test beam set ups with other tracking sub-detectors, i.e. vertex detector and TPC prototypes. In addition major contributions were provided to the LOIs of the detector concepts and now to the next steps i.e. ILC DBD and CLIC CDR expected documents in the next two years. They develop new aspects of the SiLC activities i.e. the integration studies and request stronger effort on developing the simulation tools. An important new fact is the contribution to new experiments starting in a near future as well as transnational applications of the EUDET E.U. project. It is very useful for reinforcing several aspects of this R&D and as training camp too but it is demanding a lot of dedicated efforts.
Another important new aspect is the start of an active participation to the CLIC R&D studies especially within the WG3 working group on vertex and tracking at CLIC. Again this is an asset for further developing the R&D and extending its applications. All this is successfully achieved up to now by the SiLC Collaboration as it can be seen from the number of contributions to workshops and conferences, published papers and Internal Notes (see Appendix) , and the fact that experiments are interested in our developments and are requesting our collaboration.

But SiLC is facing, as all the major R&D collaboration for the Linear collider severe restrictions in budget and manpower. This is making life harder and harder, initiating struggles for life. This makes more and more difficult to maintain such an active level of R&D as reported here. And, in addition, the work requested for these next few years is even more demanding than it was, on all the aspects!

The EUDET E.U. project demanded a lot of efforts and means to all the participating institutes but on the other hand brought a substantial financial support, job openings and access to test beam facilities. AIDA new E.U. project will not provide at all the same level of support.
The closure of SPS CERN test facility in 2012 (an especially important year for the LC project) for at least one year is another important fact. The CERN test facilities are crucial for our developments.

The extended applications of SiLC beyond the Linear Collider are very demanding in terms of work. They should hopefully provide additional funds and people and also will be somehow very valuable training camps. SiLC is bringing an instrumental contribution to the construction of these experiments with dedicated manpower and means that are somehow taken from the overall R&D line; therefore such extended applications are assets from the scientific and technological points of view but do not solve the lack of means for the LC R&D's even the contrary.

To conclude, the support in funds and manpower are becoming a very severe issue that has to be seriously addressed and confronted by all our LC community if we want to successfully achieve the milestones and somehow tight schedule of the Linear Collider program.
It is important to mention the efforts of some teams that have no means allocated in their research program for LC R&D and despite this are valuably contributing to SiLC, especially Italy (Torino) and UK (Ch. Damerell at Rutherford Lab.). This is likely to become the case in other countries if no action is taken. The lack in temporary or permanent job openings for the LC is a global crucial problem for all the R&D's for the Linear collider. The LC R&D's should be set at a much higher priority level by the funding agencies than currently in most of the countries.

APPENDIX

LIST OF PUBLICATIONS, WORKSHOPS AND CONFERENCES Where SiLC contributed, since May 2008 till October 2010

1.- WORKSHOPS & CONFERENCES

- ECFA-LC 2010 Workshop, Oct. 18-22, CERN
Several SILC presentations in preparation

- LCWS'10, Beijing, March 26-30, 2010
A. Ruiz-Jimeno, (IFCA), ''Overview of the Spanish Tracking R&D for the FLC'' http://ilcagenda.linearcollider.org/getFile.py/access?contribId=242&sessionId=13&resId=1&materialId=slides&confId=4175
A. Savoy-Navarro (LPNHE), ''Silicon Tracking for the Linear Collider: Advances, issues and perspectives''
http://ilcagenda.linearcollider.org/getFile.py/access?contribId=240&sessionId=13&resId=0&materialId=slides&confId=4175
A. Savoy-Navarro (LPNHE) ''Front End Readout and DAQ for Silicon trackers at Linear Colliders''
http://ilcagenda.linearcollider.org/getFile.py/access?contribId=241&sessionId=13&resId=0&materialId=slides&confId=4175
B. Schumm (UCSC-SCIPP), '' Fundamental microstrip R&D at SCIPP''
http://ilcagenda.linearcollider.org/getFile.py/access?contribId=306&sessionId=13&resId=1&materialId=slides&confId=4175

- Workshop on ''Muon g-2 and EDM in the LHC era'', organized by N. Saito and A. Savoy-Navarro, Paris, Feb 26, 2010, *sponsored by the Federation de recherchesInteraction Fondamentale*
http://www.lpthe.jussieu.fr/fed/E_Conf.html

- Linear Collider Test Beam Workshop, Orsay, 3-5 Nov 2009
A. Charpy (LPNHE) on behalf of the SiLC R&D collaboration, ''SiLC Test Beam Experience/Plans''
http://ilcagenda.linearcollider.org/getFile.py/access?contribId=38&sessionId=21&resId=0&materialId=slides&confId=3735
A. Savoy-Navarro (LPNHE), ''Ressources for test beams (human and funding)''
http://ilcagenda.linearcollider.org/conferenceDisplay.py?confId=3735
M.Vos (IFIC-CSIC) ''Si tracking summary''
http://ilcagenda.linearcollider.org/getFile.py/access?contribId=44&sessionId=28&resId=1&materialId=slides&confId=3735

- CLIC'09, October 12-16 2009, CERN, Geneva (CH)
M. Vos (IFIC-CSIC), ''Requirements on Forward Tracking and Tagging''
http://indico.cern.ch/getFile.py/access?contribId=178&sessionId=4&resId=0&materialId=slides&confId=45580

Ch Damerell (RAL), ''A Silicon Pixel Tracker for CLIC''
http://indico.cern.ch/getFile.py/access?contribId=255&sessionId=4&resId=1&materialId=slides&confId=45580

- 2009 Linear Collider Workshop of the Americas, Albuquerque, Sept.28-Oct 4, 2009
A. Ruiz-Jimeno (IFCA), ''Forward Tracking at the ILC''
http://ilcagenda.linearcollider.org/getFile.py/access?contribId=213&sessionId=7&resId=0&materialId=slides&confId=3461
B. Schumm (UCSC-SCIPP), ''ILC Instrumentation R&D at SCIPP''
http://ilcagenda.linearcollider.org/getFile.py/access?contribId=214&sessionId=7&resatILCId=1&materialId=slides&confId=3461
Carman Jerome (SCIPP), ''Exploration of Charge Division with Strip Detectors''
http://ilcagenda.linearcollider.org/getFile.py/access?contribId=216&sessionId=7&resId=0&materialId=slides&confId=3461
B. Schumm and A. Savoy-Navarro, ''Update from the SiLC R&D Collaboration: achievements and perspectives''
http://ilcagenda.linearcollider.org/getFile.py/access?contribId=220&sessionId=7&resId=0&materialId=slides&confId=3461
W. Mitaroff, ''Silicon Tracking in Vienna: Status report''
http://ilcagenda.linearcollider.org/getFile.py/access?contribId=221&sessionId=7&resId=1&materialId=slides&confId=3461
A. Ruiz-Jimeno, ''Development of New Microstrip Sensors Optimized for IR Laser Track Alignment''
http://ilcagenda.linearcollider.org/getFile.py/access?contribId=222&sessionId=7&resId=0&materialId=slides&confId=3461

- Seventh International "Hiroshima" Symposium on the Development and Application of Semiconductor Tracking Detectors, Aug. 29- Sept. 1 2009, Hiroshima, Japan
A.Savoy-Navarro, invited talk on: ''Silicon Tracking devices for the Future Linear Colliders'' (NIMA article, see publication List)
http://indico.cern.ch/contributionDisplay.py?sessionId=3&contribId=61&confId=48951

- XXIV International Symposium on Lepton Photon Interactions at High Energy, Aug. 17-22, 2009, Hamburg, Germany
A. Charpy, Presentation on the SiLC R&D Activities at the Poster Session

- TILC'09, joint ACFA Physics abd Detector Workshop and GDE Meeting, April 16-21, 2009, Tsukuba, Japan.
A. Ruiz-Jimeno (IFCA), ''Forward Tracking at the next e+e- collider''
http://ilcagenda.linearcollider.org/getFile.py/access?contribId=125&sessionId=26&resId=3&materialId=slides&confId=3154
A. Savoy-Navarro (LPNHE) '' Integrating Silicon Tracking in the ILC detector concepts: solutions and challenges''
http://ilcagenda.linearcollider.org/getFile.py/access?contribId=126&sessionId=26&resId=1&materialId=slides&confId=3154
A. Savoy-Navarro,'' A mixed mode chip in 130nm for Silicon Strips Readout at the Linear Collider''
http://ilcagenda.linearcollider.org/contributionDisplay.py?contribId=127&sessionId=26&confId=3154

- TIPP'09, 1st Technology and Instrumentation in Particle Physics Workshop, March 2009
Th. Bergauer (HEPHY-Vienna) ''Silicon Microstrip Detector for an ILC experiment'', Poster session
T.H.Pham (LPNHE), ''A mix mode FE readout for strip sensors for the Linear Collider in 130nm CMOS technology'' (NIMA article see publication list)

- LCWS'08, Nov 15-20, 2008, Chicago (USA)
B. Schumm (UCSC-SCIPP), ''Update on Electronic Readout Issues at SCIPP''
http://ilcagenda.linearcollider.org/getFile.py/access?contribId=214&sessionId=21&resId=1&materialId=slides&confId=2628
W. Mitarof (HEPHY), ''Tracking Detector Optimization with Fast Simulation and its application to the ILD Design'', see:
http://ilcagenda.linearcollider.org/contributionDisplay.py?contribId=217&sessionId=21&confId=2628
S. Haensel (HEPHY), ''Silicon Detectors for the Large Prototype TPC test set up at DESY''
http://ilcagenda.linearcollider.org/contributionDisplay.py?contribId=227&sessionId=21&confId=2628
A. Savoy-Navarro (LPNHE), ''Overview of the SiLC R&D activities''
http://ilcagenda.linearcollider.org/contributionDisplay.py?contribId=483&sessionId=21&confId=2628
S. Haensel (HEPHY), ''Resolution Studies on Silicon Strip sensors with fine pitch''
http://ilcagenda.linearcollider.org/contributionDisplay.py?contribId=232&sessionId=21&confId=2628
A. Ruiz-Jimeno (IFCA), ''Alignment of Silicon Tracking system: R&D and first prototypes''
http://ilcagenda.linearcollider.org/contributionDisplay.py?contribId=484&sessionId=21&confId=2628
A. Savoy-Navarro (LPNHE), ''New Front End and Readout chip for strip detector at ILC in 130n m CMOS technology''
http://ilcagenda.linearcollider.org/contributionDisplay.py?contribId=485&sessionId=21&confId=2628
A. Savoy-Navarro (LPNHE), ''Silicon Tracking DAQ'',
http://ilcagenda.linearcollider.org/contributionDisplay.py?contribId=264&sessionId=25&confId=2628

- CLIC'08, 14-17 Oct 2008, CERN
A. Savoy-Navarro, "Silicon tracking for CLIC experiments", invited talk
http://indico.cern.ch/contributionDisplay.py?sessionId=22&contribId=276&confId=30383

- ECFA-LC Workshop, June 2008, Warsaw
Several SiLC contributions on all aspects of the Tracking R&D, Alignment, DAQ and FE Electronics as well as first tests beam results.
(The Workshop Website is no more available)

Seminars:

- Seminar at the Seoul National University, March 16 2010, on *''Silicon Tracking at the future Linear Collider(s): Challenges and Synergies"* ***b***y A. Savoy Navarro (LPNHE)

A series of annual status reports from the Collaborative joint FJPPL program between KEK and LPNHE on the R&D on Silicon Tracking:

- Presentation at FJPPL-LIA, LAPP-Annecy, June 2010
A. Savoy-Navarro (LPNHE), on behalf of the D_RD_4 group, *''New Generation of Large Area Si Tracking''*

- Presentation at FJPPL-LIA, KEK, May 2009
T. Tsuboyama (KEK), on behalf of the D_RD_4 group, *''New Generation of Large Area Si Tracking''*

- Presentation at FJPPL-LIA, Paris, May 2008
A. Savoy-Navarro (LPNHE) andT. Tsuboyama (KEK), on behalf of the D_RD_4 group, *''New Generation of Large Area Si Tracking''*
See Website: http://fjppl.in2p3.fr/cgi-bin/twiki.source/bin/view/FJPPL/WebHome

- Presentation at the First Muon g-2/EDM collaboration meeting, June 8, 2010, Seminar Hall in KEK (Japan)
A. Savoy-Navarro (LPNHE) ''From SiLC to g-2''.

2.- SiLC Collaboration Meetings

Held once per year during 3 days with an intermediate Collaboration Meeting of half day, usually held at CERN

7th SiLC Collaboration Meeting at CERN, July 2nd, 2008 (intermediate meeting)

http://ilcagenda.linearcollider.org/conferenceDisplay.py?confId=2794

8th SiLC Collaboration Meeting in Santander, 17-19, Dec. 2008

http://www.ifca.unican.es/SiLC/index.html

SiLC intermediate Collaboration Meeting at CERN, during CLIC'09.

9th SiLC Collaboration Meeting in Paris, Jan. 2010

http://lpnhe.in2p3.fr/spip.php?rubrique127

3.- EUDET Annual Meetings:

Held once per year, in October; It includes a plenary session with ½ hour presentation of the SiTRA activity during the past year and achieved SiTRA objectives. It also includes a 2 hour parallel session dedicated to the activities of the SiTRA-JRA2 workpackage:

EUDET Annual Collaboration Meeting (Final), Sept 2-Oct 1, 2010, DESY
Parallel Session, SiTRA task *chaired by A. Savoy-Navarro*
Contributions from:

- ⇨ Prague Transnational Activity on TileCal
- ⇨ Juha Kallopuska (VTT) on new batch of Edgeless strip sensors from VTT
- ⇨ Jacques David (LPNHE) on the SiTRA standalone and Multipurpose test infrastructure
- ⇨ Alexandre Charpy (LPNHE) on the transnational applications of the test beams in May and November 2010 at CERN
- ⇨ Marcos Fernandez (IFCA) on the IR transparent strip sensors developments

Al the slides are in:

http://ilcagenda.linearcollider.org/sessionDisplay.py?sessionId=16&slotId=0&confId=4649#2010-09-29

Plenary session on JRA2:

A. Savoy-Navarro on behalf of the SiTRA-JRA2 group, ''SiTRA-JRA2 Activity: achievements and outcomes'', See:
http://ilcagenda.linearcollider.org/materialDisplay.py?contribId=118&sessionId=21&materialId=slides&confId=4649

- EUDET Annual Collaboration Meeting, Oct 19-21, 2009, Univ. Geneva/CERN

Parallel Session, SiTRA task *chaired by A. Savoy-Navarro*

Contributions from:

- ⇨ Th. Bergauer (HEPHY): SPS test beams with the HEPHY test system
- ⇨ M. Fernandez (IFCA): Advances on the new friendly alignment sensors
- ⇨ A. Savoy-Navarro (LPNHE): Standalone Silicon test system and Transnational Aspects
- ⇨ T.H. Pham (LPNHE): The SiTR chip present results and new version

All slides are in:
http://ilcagenda.linearcollider.org/sessionDisplay.py?sessionId=8&slotId=0&confId=4127#2009-10-19

Plenary session on JRA2:

I, Vila (IFCA) on behalf of the SiTRA-JRA2 group, ''SiTRA task status report''
http://ilcagenda.linearcollider.org/contributionDisplay.py?contribId=27&sessionId=15&confId=4127

- EUDET Annual Collaboration Meeting, Oct 6-8 2008, NIKHEF

Parallel Session, SiTRA task *chaired by I. Vila*

Contributions from:

- ⇨ S. Haensel (HEPHY): Progress Report on the Silicon Detectors for the LC-TPC combined test
- ⇨ P. Kvasnicka (CU Prague): SiLC test beam at CERN, June 2008
- ⇨ M. Fernandez (IFCA): Alignment of Si tracking system: R&D and first EUDET prototype
- ⇨ A. Charpy (LPNHE) SiTRA test beams at CERN: infrastructure developments and results
- ⇨ T.H. Pham (LPNHE) The new front-end readout chip for Si microstrips in DSM CMOS technology

All slides are in:
http://ilcagenda.linearcollider.org/sessionDisplay.py?sessionId=11&slotId=0&confId=2811#2008-10-06

Plenary session on JRA2:

A. Savoy-Navarro on behalf of the SiTRA-JRA2 group, ''SiTRA-JRA2 task status report'' ac
See:
http://ilcagenda.linearcollider.org/sessionDisplay.py?sessionId=22&slotId=0&confId=2811#2008-10-07

4.- ILD Concept Group General Meetings

ILD Software and Integration Meeting, June 2010
Contributions from Alexandre Charpy (LPNHE), J. Duarte (IFCA) and W. Mitarof (HEPHY) in the ILD software session and from A. Savoy-Navarro in the ILD Integration session.

Annual Meeting, Jan 28-30, 2010, Paris
A, Savoy-Navarro (LPNHE), on behalf of the SiLC members participating to the ILD concept, ''Silicon Tracking for the ILD'' in the R&D contributions; see:
http://ilcagenda.linearcollider.org/getFile.py/access?contribId=11&sessionId=24&resId=0&materialId=slides&confId=4326
J. Duarte (IFCA), ''Forward Tracking'', in the optimisation session, See:
http://ilcagenda.linearcollider.org/contributionDisplay.py?contribId=29&sessionId=28&confId=4326

Annual Meeting, Feb 16-18 2009, Seoul
A, Savoy-Navarro (LPNHE), on behalf of the SiLC members participating to the ILD concept, ''Silicon Tracking for the ILD'', in the plenary session; see:
http://ilcagenda.linearcollider.org/getFile.py/access?contribId=3&sessionId=25&resId=0&materialId=slides&confId=3159
M. Vos (IFIC), ''Forward Tracking: physics case, challenges and design''; See:
http://ilcagenda.linearcollider.org/getFile.py/access?contribId=61&sessionId=44&resId=0&materialId=slides&confId=3159

5.- WG3 CLIC Working Group

Contributions given on:
- Very Forward Detector and Physics Studies (IFIC, BU and IFCA)
- Time Stamping at CLIC (LPNHE)
- Description of the Silicon tracking geometry in detailed simulations (LPNHE)

6.- PUBLICATIONS

6.1- Published papers

- A. Savoy-Navarro, *'Development of Semi Conductor tracking: the future linear collider case',* Nucl. Instr. And Meth. A, 51508, article in press
- T. H. Pham, *'A 130nm mixed mode FE readout chip for Si strip tracking at the Future Linear Collider',* Nucl. Instr. And Meth. A., article in press
- The International Large Detector LOI, by the ILD Concept Group, Feb. 2010, DESY 2009-87, FERMILAB-PUB-09-682-E, KEK Report 2009-6.
- The Silicon Detector Concept LOI, by the SiD Concept Group, March 31, 2009.

And a number of publications in Proceedings:
Proceedings of LCWS'10 (to appear)
of LCWS'08 (list corresponds to the various contributions listed in 1.-)
of TIPP'09…

(List of publications not complete yet)

6.2- EUDET-Memos

- List of memos in 2010:

About 10 EUDET memos expected and in preparation for the achievements in the final year of the EUDET project. It concerns the various R&D objectives, the test beams results and the transnational actions in 2010. In addition a review report is in preparation on the overall ''SiTRA-JRA2 activities, the achievements and the perspectives'' following the presentation at the plenary session at the Final EUDET Meeting.

- List of memos in 2009:

Eudet-Memo-2009-23 Final production of novel IR-transparent microstrip silicon sensors, by M.Fernandez, J.Gonzalez, R.Jaramillo et al.

Eudet-Memo-2009-22 The Silicon Tracking System: Mechanical Integration and Alignement, by A. Charpy (On behalf of the SiLC Collaboration)

Eudet-Memo-2009-21 JRA2-SiTRA: NEW VERSION OF THE MIXED MODE SILICON STRIP FRONT END AND READOUT ASIC, by T.H.Pham, A.Charpy, C.Ciobanu et al.

Eudet-Memo-2009-20 JRA2 SITRA Silicon Tracking -2009 Achievements, by SiLC Collaboration

Eudet-Memo-2009-18 Silicon Strip Sensors with integrated pitch adapters, by T.Bergauer, G. Auzinger, M.Dragicevic et al.

Eudet-Memo-2009-17 Test Beam with Silicon Detectors around the Large TPC Prototype, by S.Haensel, T.Bergauer, M.Dragicevic et al.

- List of memos in 2008:

Eudet-Memo-2008-56 JRA2 SITRA Silicon Tracking Infrastructure, M.Lozano, G.Pellegrini, E.Cabruja et al.

Eudet-Memo-2008-55 JRA2 SITRA Conductive Cooling System Prototype, A.Savoy Navarro, A.Galkin, V.Saveliev

Eudet-Memo-2008-54 JRA2 SITRA Forward Tracker Prototype, M.Lozano, G.Pellegrini, E.Cabruja et al.

Eudet-Memo-2008-37 Experimental validation of optical simulations for microstrip detectors, M.Fernandez, J.Gonzalez, R.Jaramillo et al.

Eudet-Memo-2008-28 Silicon Strips Detectors Readout ASICs in Deep Sub-Micron CMOS Technology, J-F.Genat, T-H.Pham, A.Savoy-Navarro et al.

Eudet-Memo-2008-16 Silicon Detectors for the LPTPC Test Beam, S.Haensel, T.Bergauer, M.Dragicevic et al.

Eudet-Memo-2008-15 Resolution studies on silicon strip sensors with fine pitch, T.Bergauer, Z.Dolezal, M.Dragicevic et al.